

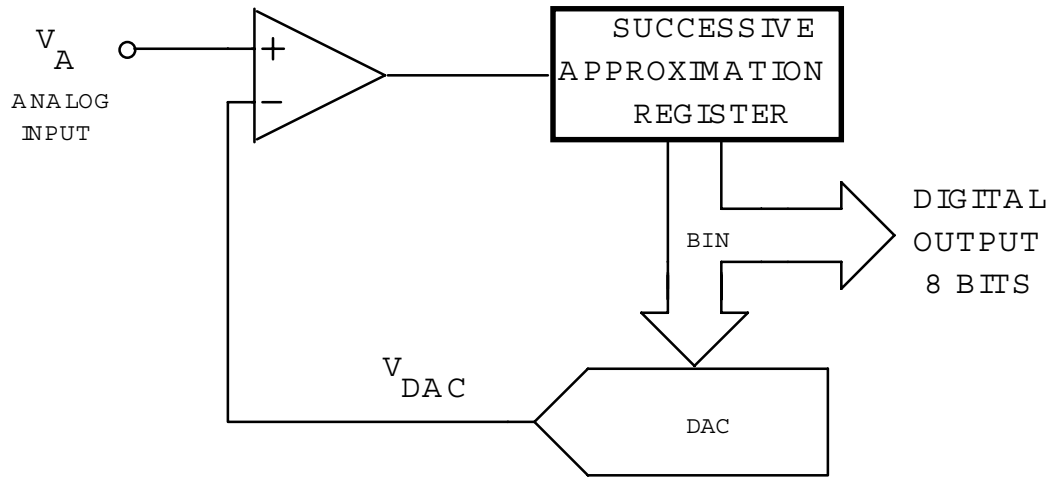
ELECTRONICS 3

EXERCISE

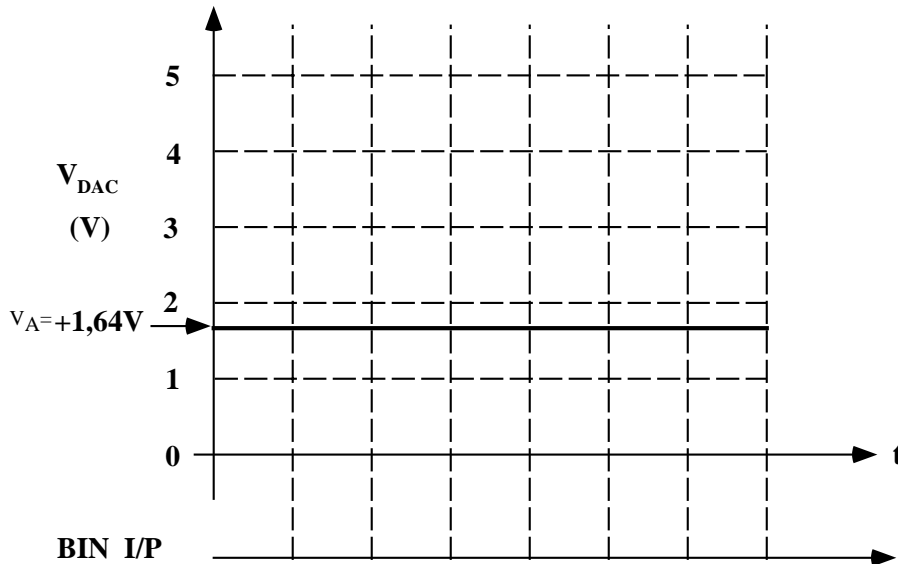
ANALOG-TO-DIGITAL CONVERTERS (ADC)

No.1

The DAC used in the ADC shown below has 8 bits and a conversion range of 0 to 5,1V.



- A) Draw the ADC transfer curve (BIN versus V_A) showing all relevant values.
- B) If $V_A=1,64V$, draw the DAC output (label all levels) and its binary input for the first five bits tested.
Hint: calculate the weight of each bit.



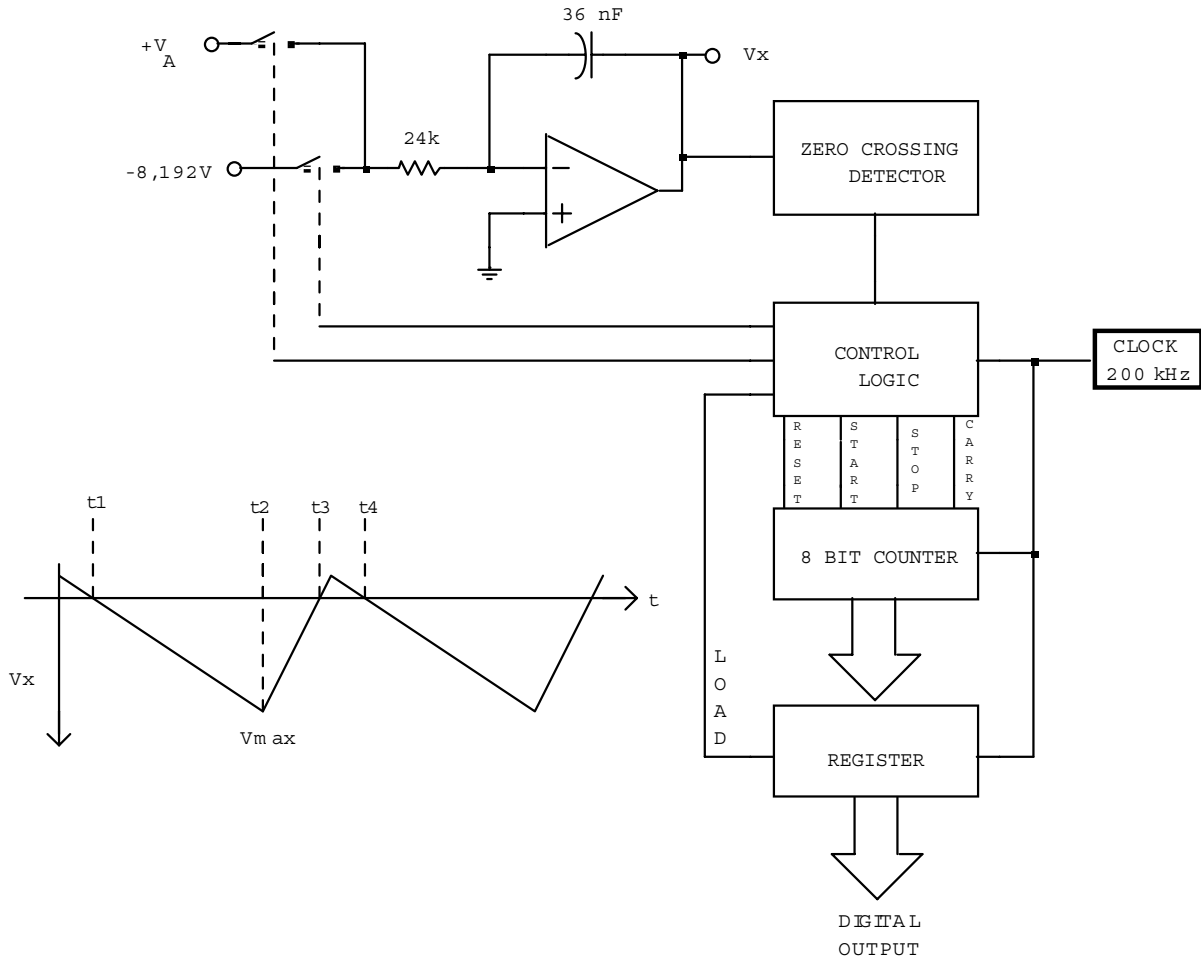
- C) What is the main advantage of this converter over the counter type ADC?

No.2

- A) Draw the block diagram of a tracking ADC and explain how it works.
- B) Explain what the maximum tracking rate (or slew rate) is and what limitation it puts on the input signal.

No.3 Draw the block diagram of a counter type ADC and explain how it works.

No.4 DUAL SLOPE ADC



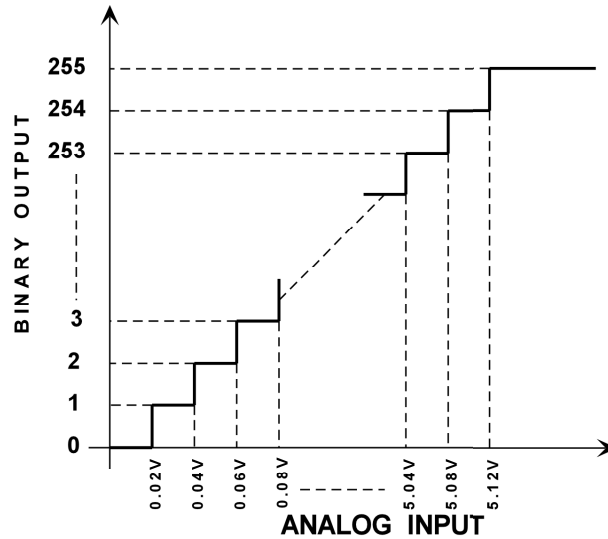
- A) Explain what happens in the ADC during the following time intervals: t_1-t_2 , t_2-t_3 and t_3-t_4 .
- B) Calculate the resolution in mV and the conversion range then draw the ADC transfer curve showing all relevant values.
- C) Prove that the digital output is given by $BIN = \frac{V_A}{V_{REF}} 2^N$.
- D) Calculate the largest value of V_{max} and the corresponding t_1-t_2 interval.
- E) Explain what makes this converter very accurate.

SOLUTIONS

No.1

A) Resolution=range/(2^N-1)=5,1/(2⁸-1)= 20 mV

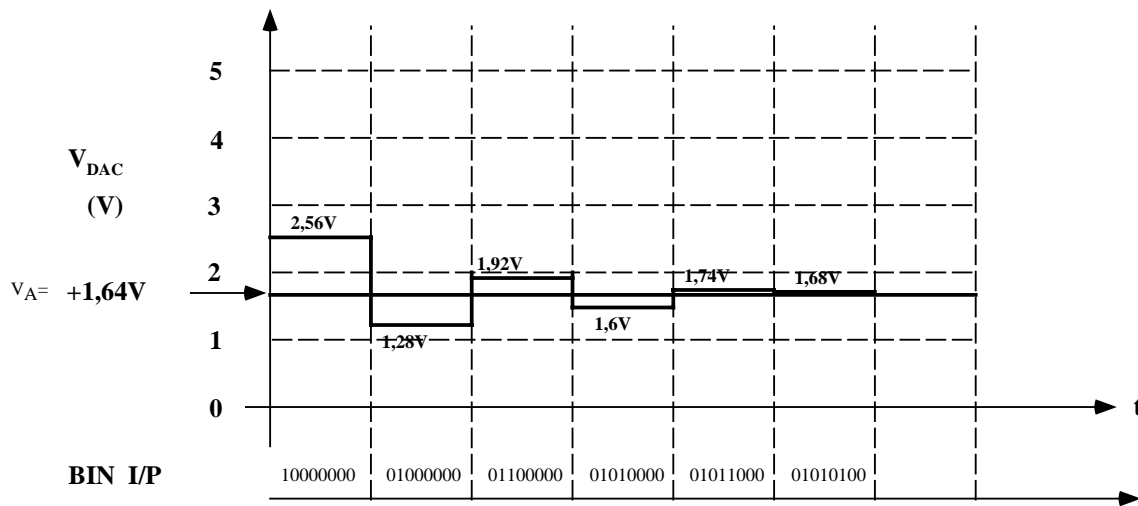
ADC TRANSFER FUNCTION



B) Calculation of bit weights

B₀=20 mV, B₁=40 mV, B₂=80 mV, B₃=160 mV, B₄=320 mV, B₅=640 mV, B₆=1,24V, B₇=2,56V

BIT TESTED	BINARY INPUT	V _{DAC} (V)	COMP. O/P	TESTED BIT IS
B ₇	10000000	2,56	LOW	LOW
B ₆	01000000	1,28	HIGH	HIGH
B ₅	01100000	1,28+0,64=1,92	LOW	LOW
B ₄	01010000	1,28+0,32=1,6	HIGH	HIGH
B ₃	01011000	1,28+0,32+0,16=1,74	LOW	LOW
B ₂	01010100	1,28+0,32+0,08=1,68	LOW	LOW



C) It is a much faster converter than the counter type converter.

SAR: $T_{conv} = N/F_{clk}$ (fixed) COUNTER: $T_{conv} = 0 \text{ to } (2^N-1)/F_{clk}$ (variable)

Where N is the number of bits. For small voltages, the counter type ADC is faster but for most of the range, it is slower.

No.2 See theory notes

No.3 See theory notes

No.4 DUAL SLOPE ADC

A) t_1-t_2 : V_A is switched in, slope= $-V_A/(RC)$, counter counts from 0 to 255 and resets automatically to 0 on the 256th clock pulse. $t_2-t_1=256/F_{clk} = 1,28 \text{ ms}$. At t_2 , the reference voltage is switched in and the analog voltage switched out.

t_2-t_3 : slope= $+V_{ref}/(RC)=+8.192/(24k*36n)=9481,5V/s$. Counter counts from 0 to BIN where BIN is the final count or conversion.

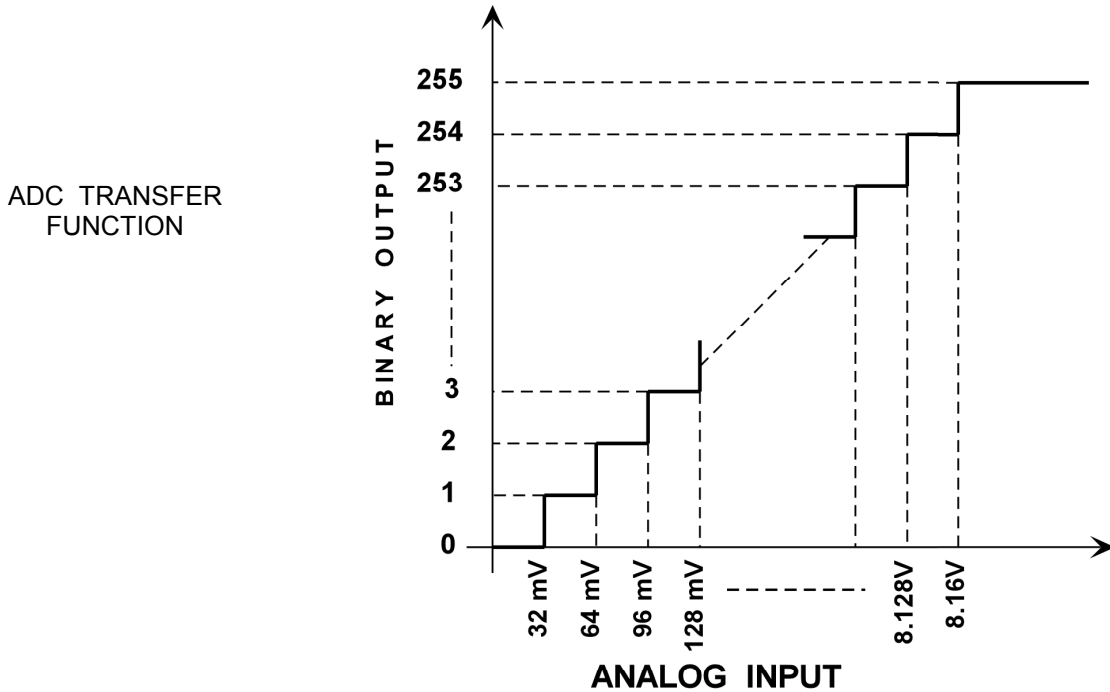
t_3-t_4 : BIN is transferred to register, counter is reset, $-V_{ref}$ is switched out and $+V_A$ is switched in for the next conversion.

The zero crossing detector tells the control logic when to start or stop the counter.

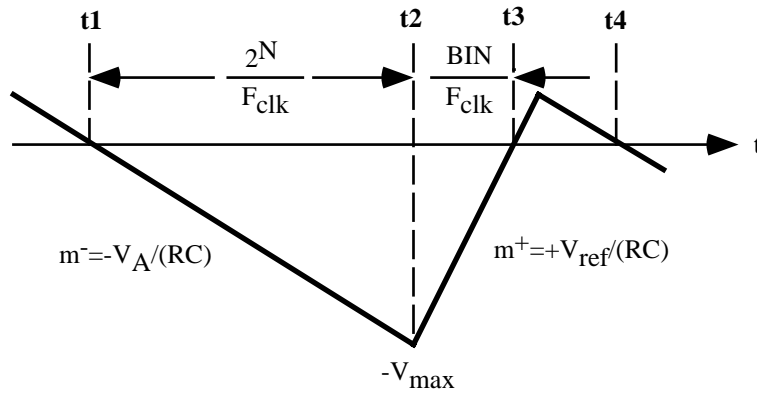
B) $V_A = \text{BIN} * V_{ref}/2^N$ BIN= 0 to 2^N-1

conversion range: $V_A = (0 \text{ to } 255) * 8,192/256 = 0 \text{ to } +8,16V$

Resolution: V_A for BIN=1 res.= $1 * 8,192/256 = 32 \text{ mV}$



C)



$$\left| \frac{m^-}{m^+} \right| = \frac{\frac{V_A}{RC}}{\frac{V_{REF}}{RC}} = \frac{\frac{V_{MAX}}{2^N / F_{CLK}}}{\frac{V_{MAX}}{BIN / F_{CLK}}}$$

$$\frac{V_A}{V_{REF}} = \frac{BIN}{2^N} \Rightarrow BIN = \frac{V_A}{V_{REF}} 2^N$$

D) The largest value of $(t_2 - t_1)$ occurs for $V_A \max = 8,16V$

$$m^- = \frac{-V_A}{RC} = \frac{-V_{\max}}{2^N} F_{clk}$$

$$V_{\max} = \frac{-V_A}{RC} \frac{2^N}{F_{clk}} = -\frac{8,16}{24k * 36n} \frac{2^8}{200k} = -12,09V$$

$$t_2 - t_1 = 2^8 / 200k = \underline{1,28 \text{ ms}}$$

E) The conversion does not depend on F_{clk} , R and C , therefore the accuracy of the conversion depends mainly on the precision of V_{ref} . R , C and F_{clk} have to be stable only on a short term basis. One can also demonstrate that the zero crossing detector's DC offset does affect the accuracy of the conversion either.