

## PROGRAMMABLE POWER SUPPLY PRE-LAB INSTRUCTIONS

- Provide a circuit diagram with your final standard component values.  
I will not correct a pre-lab without a circuit diagram.
- State all component specifications used in your design and explain your reasoning.

### 1. VOLTAGE LOOP

- Calculate R7 first for the desired O/P voltage and a reasonable DAC-1 O/P current.
- Once R7 has been selected, determine  $I_{REF1}$  then calculate the reference branch resistors.
- Calculate R6 to obtain enough  $V_{GS}$  drive level to provide the maximum load current. Pick a reasonable current value for  $I_6$  max. Don't forget to include the 1.1V voltage drop, that is  
 $V_{R6} = V_{SG} + 0.5 * I_L * 1.1$
- R4 and R5 provide feedback to Q3 and help stabilize the feedback loop. They must be calculated such as to ensure that  $V_{o1}$  does not saturate. The worst case  $V_{R5}$  max occurs when  $V_o$  and  $I_L$  are both max.  $I_{R5} \text{ max} = I_{E3} \text{ max} + I_{R4} \text{ max} = V_{R6} \text{ max} / R_6 + I_{R4} \text{ max}$  Assume a reasonable value for  $I_{R4} \text{ max}$  to limit power dissipation below 100 mW in R4.

### 2. SUBTRACTOR

- Pick gain of subtractor such as to maximize  $V_{o2} \text{ max}$  without risking saturation of A2. A high  $V_{o2}$  will minimize the DC offset effects of the op amps and will make the current limit more accurate.
- Select standard R1 and R3 for desired gain and calculate  $V_{o2} \text{ max}$  with std R values and use that  $V_{o2}$  value to design the second DAC circuit. Calculate R2 to attenuate the subtractor input voltages within the worst case op amp I/P voltage range.
- Select  $V_2^+$  and  $V_2^-$  max as high as possible without getting too close to the limit. This will maximize the value of R2 and make matching of R2's less critical.

### 3. DAC-2 DESIGN

- select standard R10 first for desired  $V_{o4} \text{ max} = V_{o2} \text{ max}$  and reasonable  $I_{DAC2}$ .
- Calculate  $I_{REF2}$  and then calculate reference branch resistors.

### 4. 2.5V REFERENCE

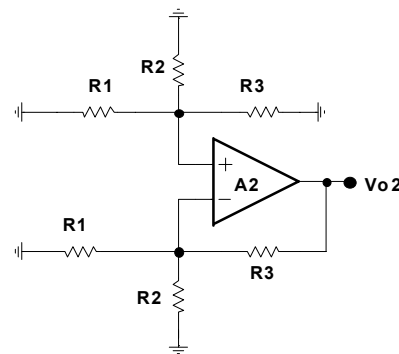
Calculate the biasing resistor (above LM4040B) small enough to supply the two DAC reference currents and a minimum of 1.5 mA to the LM4040B. Don't pick resistor too large as you may exceed current bias of LM4040B – see spec's for max current.

### 5. CAPACITORS

Calculate all caps as per procedure instructions.

To calculate the BW of the subtractor, you have to find  $\beta_V$  and then use  $BW = \beta_V * GBW$  of LF411

To find  $\beta_V$ , you have to ground all DC sources and also ground the two subtractor inputs as shown beside, then find  $\beta_V = V^- / V_0$



### 6. RESISTOR R8

When the diode conducts the load is current limited and  $I_{R8} = I_{DAC1} - I_{R7} = I_{DAC1} - V_o / R_7$  where  $V_o$  is the load voltage which is no longer regulated (see page 7 of lab sheets for load regulation characteristics). For current limiting to remain effective, the O/P of A3 must not saturate in order to keep the inputs of A3 forced equal.  $V_{o3}$  will be maximum when  $V_o$  is 0V, that is in a short circuit condition ( $R_L = 0$ ).  $I_{R8} \text{ max} = I_{DAC1} = I_{REF1} * BIN_1 / 256$ .

Select  $R_8$  such that  $V_{o3} = I_{R8} \text{ max} R_8 + V_{DF}$  does not get too close to the worst case saturation voltage.