P R O G R A M M A B L E P O W E R S U P P L Y

PRE-LAB

Design a programmable power supply that meets the following specifications.

CASE #	Unregulated V_{in} (V)		V_o max (V)	I_{LIMIT} max (A)	5% std resistors
	min	max	BIN1=255_{dec}	BIN2=100_{dec}	X 10^N
1	18	22	15.3	1.5	1
2	18.5	22.5	15.81	1.45	1.1
3	19	23	16.32	1.4	1.2
4	19.5	23.5	16.83	1.35	1.3
5	20	24	17.34	1.3	1.5
6	20.5	24.5	17.85	1.25	1.6
7	21	25	18.36	1.2	1.8
8	21.5	25.5	18.87	1.15	2
9	22	26	19.38	1.1	2.2
10	22.5	26.5	19.89	1.05	2.4
11	23	27	20.4	1	2.7
12	23.5	27.5	20.91	0.95	3
13	24	28	21.42	0.9	3.3
14	24.5	28.5	21.93	0.85	3.6
15	25	29	22.44	0.8	3.9
16	25.5	29.5	22.95	0.75	4.3
17	26	30	23.46	0.7	4.7
18	26.5	30.5	23.97	0.65	5.1
19	27	31	24.48	0.6	5.6
20	27.5	31.5	24.99	0.55	6.2
21	28	32	25.5	0.5	6.8
22	28.5	32.5	26.01	0.45	7.5
23	29	33	26.52	0.4	8.2
24	29.5	33.5	27.03	0.35	9.1

Available Capacitors: 150 pF, 220 pF, 750 pF, 3.3 nF, 33 nF and 0.33 µF

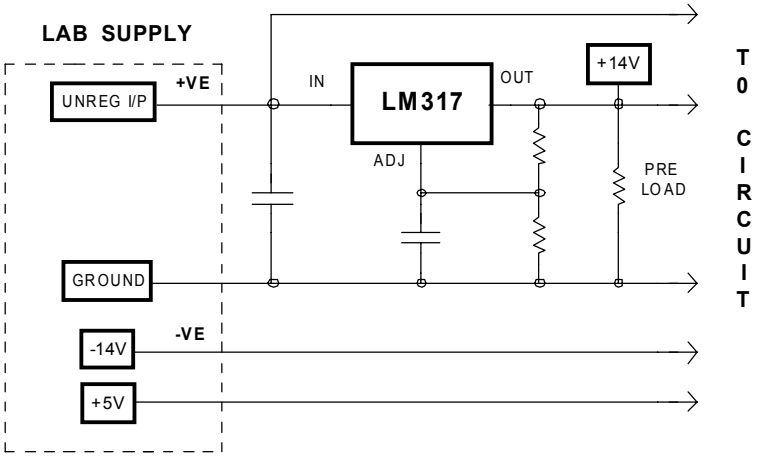
CALCULATION OF CAPACITORS

Select C_1 on test for stable voltage loop - range 1nF to 0,1 µF. The smaller C_1 is, the faster the regulated output voltage will react to transient changes, but if it is too small the feedback loop risks being unstable for certain load currents.

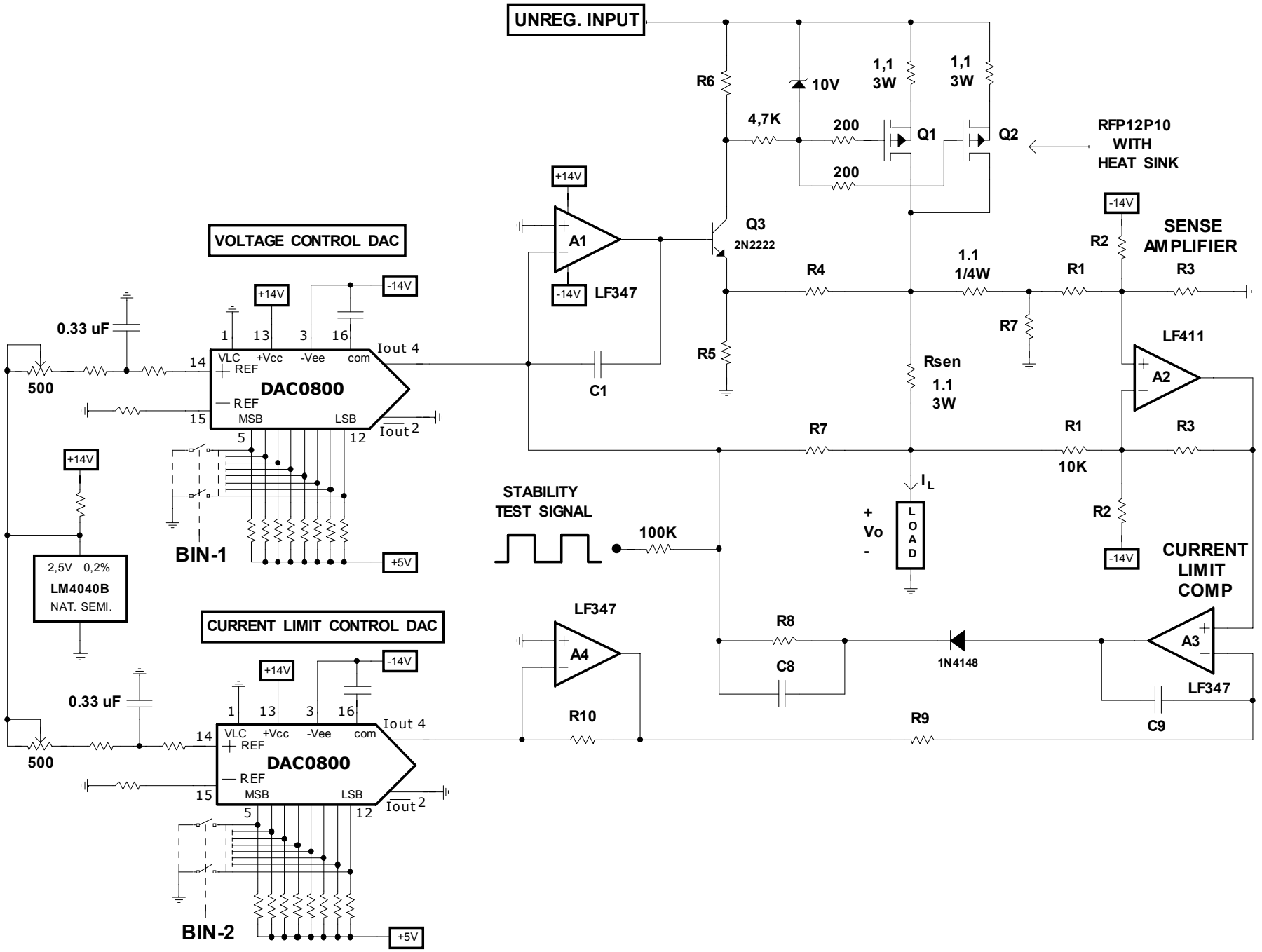
Calculate C_8 such that $(2\pi R_8 C_8)^{-1} = BW_{SUB}$

Calculate C_9 R_9 such that $(2\pi R_9 C_9)^{-1} \approx 500$ Hz

A small 0,01 to 0,1 µF cap across the load may have to be used for stability..



Use an LM317 to produce the +14V supply voltage.


UNREG. INPUT
R6
10V
1,1
3W
1,1
3W
4,7K
200
Q1
Q2
RFP12P10
WITH
HEAT SINK
200
+14V
A1
-14V
LF347
Q3
2N2222
-14V
SENSE
AMPLIFIER
R2
R4
1.1
1/4W
R1
R3
R7
LF411
A2
R5
Rsen
1.1
3W
C1
VOLTAGE CONTROL DAC
0.33 uF
500
+14V
-14V
1
13
3
16
14
VLC
+Vcc
-Vee
com
REF
DAC0800
REF
15
MSB
LSB
5
12
Iout 4
Iout 2
+5V
BIN-1
+14V
2,5V 0,2%
LM4040B
NAT. SEMI.
R7
R1
R3
10K
R2
-14V
I_L
+
Vo
-
LOAD
STABILITY
TEST SIGNAL
100K
CURRENT
LIMIT
COMP
LF347
A4
R8
C8
1N4148
A3
LF347
C9
CURRENT LIMIT CONTROL DAC
0.33 uF
500
R10
R9
BIN-2

PROCEDURE

C A U T I O N

Monitor V_o all the time on the scope to ensure that there are no oscillations – an unstable feedback loop will oscillate, change the stabilising capacitor values to stop the oscillations.

Do not operate the load at I_{max} for too long because the heat sinks are marginal for the amount of power being dissipated.

Part 1 VOLTAGE-CONTROL LOOP

1. Measure the precision reference voltage and the LM317 output voltage. Check for absence of HF oscillations at LM317 output – use scope.

V_{ref}		V_{out} of LM317	
Expected	Measured	Expected	Measured

2. Calibrate the voltage control DAC for an accurate full scale voltage without any load – you may have to change one of the fixed resistors in the DAC +ref branch if the pot does not provide enough range.

V_{FS} = _____ State resistor change (if any):_____

3. Stability test

Set BIN1 to 128 and verify the voltage loop stability by observing the transient response of V_o resulting from the squarewave test signal shown on the circuit diagram – use 4 V_{PP} and a long enough period such that the output transient waveform has time to stabilise.

Verify that loop is stable (no ringing on V_o, only exponential edges) for I_L = 0 to 90% of I_{Lmax}
If ringing occurs, increase C_1 until it oscillations disappear.

Measure the (10%-90%) loop rise and fall times (V_O waveform) for I_L = 0, I_L = 50% of I_{Lmax} and I_L = 90% of I_{Lmax} using the same test squarewave.

I_L = 0		I_L = 50% of I_{Lmax}		I_L = 90% of I_{Lmax}	
Rise time	Fall time	Rise time	Fall time	Rise time	Fall time

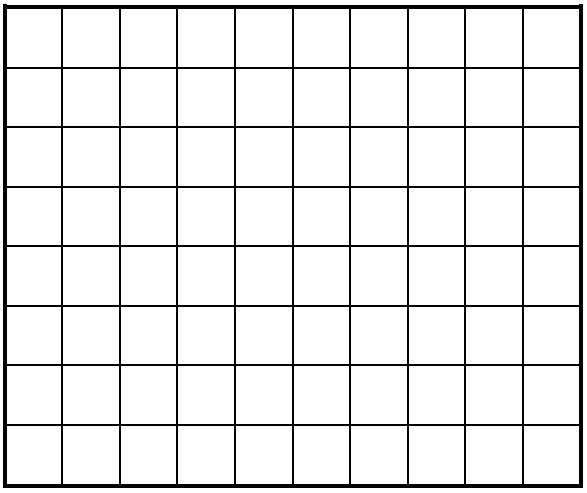
Did the loop speed change with different load currents? Explain.

_____

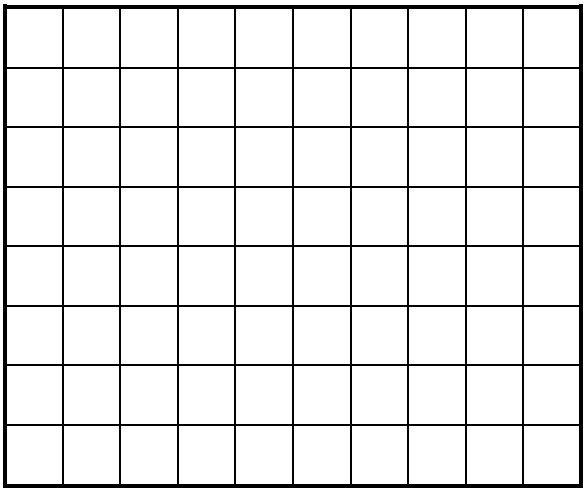
_____

Teacher demo: Record the output waveform when the loop is unstable and compare to the stable loop response.

Stable O/P waveform



Unstable O/P waveform



4. Measure all bit weights and V_{FS} without a load.

	BIT WEIGHT	
BIT	**Expected**	**Measured**
B_o (LSB)		
B_1		
B_2		
B_3		
B_4		
B_5		
B_6		
B_7 (MSB)		

V_{FS}	
Expected	Measured

5. Measure V_{FS} no load and full load then calculate the % load regulation. To do so, set decade box R value to obtain about I_L = 95% of I_{Lmax} and then toggle decade box last knob from 0 to 100K every 3 or 4 seconds so that you don't measure drift of V_o. If % regulation is not less than 0,05%, then clean up your grounds and measure at the proper sense point (right at the top of R_7) in the circuit.

$$LOAD\ REGULATION = \frac{V_{NL} - V_{FL}}{V_{NL}} \times 100 \ = \ \_\_\_\_\_ \text{ X } 100 = \_\_\_\_\_$$

6. Measure line regulation by varying the unregulated input voltage from the minimum to the maximum values you have been assigned and record the changes in V_o. Again this must be done fast so that you don't measure drift.

$$\text{LINE REGULATION} = \frac{\Delta V_o}{\Delta V_{in}} \times 100 \ = \ \_\_\_\_\_ \text{ X } 100 = \_\_\_\_\_$$

7. With BIN_1 = 128 and BIN_2=100, measure the minimum unregulated input voltage (V_{in}) at I_L = 0 and at I_L = 90% of I_{Lmax}, without going into current limiting, where V_o just starts dropping. Calculate the differential dropout voltage for each load condition and explain the results.

Load condition	I_L = 0		I_L = 90% of I_{Lmax}	
Dropout Voltage	**V_{in} min**	**V_{in}-V_o min**	**V_{in} min**	**V_{in}-V_o min**
Measured value				

8. Measure V_{O1} max and V_{GS} max under a worst case scenario? Also measure V_{GS} min at no load condition – this should be close to the threshold voltage of the MOSFET.

Explain worst case scenario: _____

V_{O1} max		**V_{GS} max**		**V_{GS} min at I_L = 0A**	
expected	measured	expected	measured	expected	measured

Are the above results safe? _____

_____

_____

Part II CURRENT LIMITING CONTROL LOOP

Throughout this experiment always monitor V_O on the scope to ensure that there are no oscillations.

1. **Without a load** – that is I_L = 0A - set BIN1 to 255 and then switch the MSB of BIN1 back and forth and measure the subtractor output, it should not be more than ½ LSB_2 and should not change by more than ½ LSB_2.
If the output changed by more than ½ LSB_2 your resistors are not well matched, therefore match them better and test again. If the output changed by less than ½ LSB_2 but was more than ½ LSB_2 by itself, resistors are well matched but the DC offset of the op amp is too high, you need to insert a balancing network and re-test.

NOTE: LSB_2 refers to the resolution of DAC_2 which corresponds to the weight of LSB_2. Voltage wise, $LSB_2 = V_{o4}$ produced by $BIN_2 = 1$.

2. Set BIN1 to 255 and the current limit to 10% of I_{Lmax} and decrease the load resistor until the circuit goes into current limiting and the voltage drops to about 50% of $V_o$reg and verify the current loop stability by observing the transient response of V_o resulting from the squarewave test signal shown on the circuit diagram – use 4 V_{PP} and a long enough period such that the output transient waveform has time to stabilise. Modify C_8 or C_9 if the transient response is not stable. Repeat the procedure for I_{LIM} = 90% of I_{Lmax}

With C_8 and C_9 values that make loop stable for both current limits, measure the O/P waveform rise and fall times for I_{LIM} = 10% of I_{Lmax}, and for I_L = 90% of I_{Lmax} using the same test squarewave.

I_L = 10% of I_{Lmax}		I_L = 90% of I_{Lmax}	
Rise time	Fall time	Rise time	Fall time

Did the loop speed change with different load currents? Explain.

_____

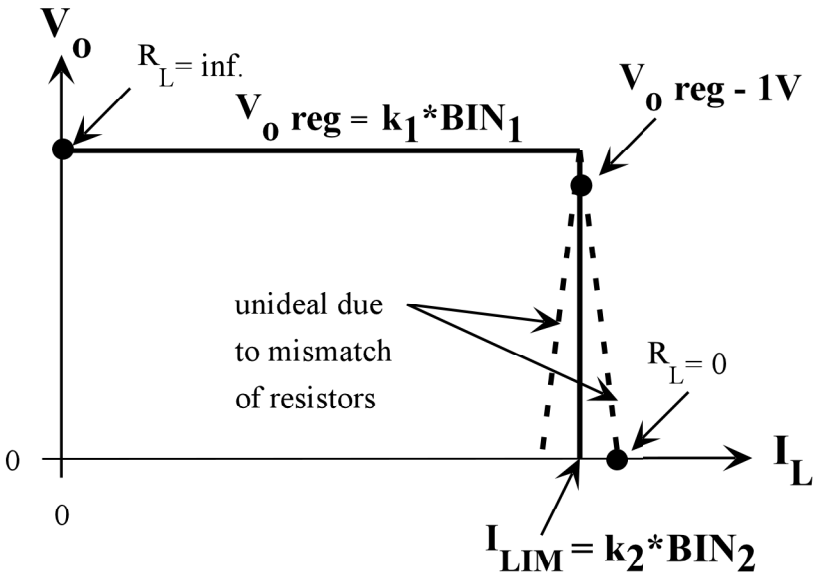
_____

Teacher demo: Record the output waveform when the loop is unstable and compare to the stable loop response.

Stable O/P waveform

Unstable O/P waveform

4. With BIN_1 remaining at 255, measure weights of bits B_0 through B_6 of BIN_2 for $V_o = V_{o\ reg} - 1V$ and and V_o=0V (R_L=0) **by decreasing R_L** until you go into current limiting. Insert a DC ammeter in series with the load to measure the actual bit weights of current limit.



"Load regulation characteristic"

	BIT WEIGHTS OF BIN_2 (I_{LIMIT})		
BIT (BIN_2)	**Expected (mA)**	**Measured at $V_{o\ reg}$ – 1V**	**Measured at V_o = 0V**
B_o (LSB)			
B_1			
B_2			
B_3			
B_4			
B_5			
B_6			
B_7 (MSB)	**Do not measure, excessive current**		

5. Measure I_{LIM} for $BIN_2 = 100_{dec}$ for $V_o = V_{o\ reg} - 1V$ and V_o=0V (R_L=0). Do not operate MOSFET's for too long at I_{Lmax} as they may overheat.

$BIN_2 = 100_{dec}$ I_{LIM} = _____ at $V_o = V_{o\ reg} - 1V$

I_{LIM} = _____ at V_o = 0V or (R_L=0)