

**PROGRAMMABLE FREQUENCY WINDOW DETECTOR .**

**PRE-LAB**

Design a programmable frequency window detector that meets the following specifications.

The circuit must accept signal levels ranging from 100 mV<sub>P</sub> to 10 V<sub>P</sub>, whether sinewaves, squarewaves or else are used as input signals. The op amps are LF347's and the voltage comparators are LM339's.

The circuit is to detect a frequency between F<sub>min</sub> and F<sub>max</sub> programmable in steps ΔF with a DAC within a window of frequency WIN-1 or a window of frequency WIN-2. Using your assigned values, determine the binary range of the DAC and its analog voltage range according to the V to F output. Note that the DAC is not used over its entire range and may be allowed to saturate at full scale. The upper and lower limits of the frequency window should be accurate to ½ LSB or ½ ΔF – this means that the O/P Schmitt triggers should have very little hysteresis but enough to overcome the maximum ripple voltage coming out of the V to F converter filter.

#	F <sub>min</sub>	F <sub>max</sub>	ΔF	WIN-1	WIN-2	F to V	#	F <sub>min</sub>	F <sub>max</sub>	ΔF	WIN-1	WIN-2	F to V
	Hz	Hz	Hz	Hz	Hz	V <sub>max</sub>		Hz	Hz	Hz	Hz	Hz	V <sub>max</sub>
1	500	5500	50	250	500	5.50	13	1540	8540	70	350	700	8.54
2	660	6660	60	300	600	6.66	14	1840	9840	80	400	800	9.84
3	840	7840	70	350	700	7.84	15	2160	11160	90	450	900	11.16
4	1040	9040	80	400	800	9.04	16	1250	6250	50	250	500	6.25
5	1260	10260	90	450	900	10.26	17	1560	7560	60	300	600	7.56
6	750	5750	50	250	500	5.75	18	1890	8890	70	350	700	8.89
7	960	6960	60	300	600	6.96	19	2240	10240	80	400	800	10.24
8	1190	8190	70	350	700	8.19	20	2610	11610	90	450	900	11.61
9	1440	9440	80	400	800	9.44	21	1500	6500	50	250	500	6.50
10	1710	10710	90	450	900	10.71	22	1860	7860	60	300	600	7.86
11	1000	6000	50	250	500	6.00	23	2240	9240	70	350	700	9.24
12	1260	7260	60	300	600	7.26	24	2640	10640	80	400	800	10.64

**Available 5% standard resistors**

1	1.2	1.5	1.8	2.2	2.7	x 10 <sup>N</sup> N = 0,1,2,3 ...
3.3	3.9	4.7	5.6	6.8	8.2	

**Available capacitors:** 2.2 nF, 3.3nF, 33 nF, 100 nF and 330 nF

**Available pots:** two 500Ω pots for the entire circuit – see circuit diagram on next page.

Supply a circuit diagram with all standard resistor values labeled directly on the diagram. You combine two standard values to make up one resistor three times at the most. Provide all of your work for the pre-lab.

**TEST PROCEDURE**

You are to provide your own test procedure and document all test results as you proceed. At the circuit demo, you must provide all test data in neat format and be able to reproduce any test data.

Circuit Diagram

