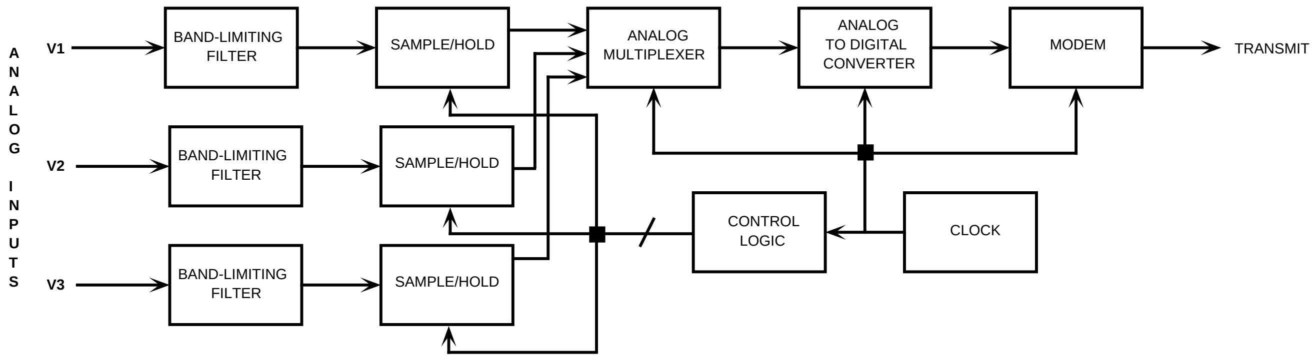
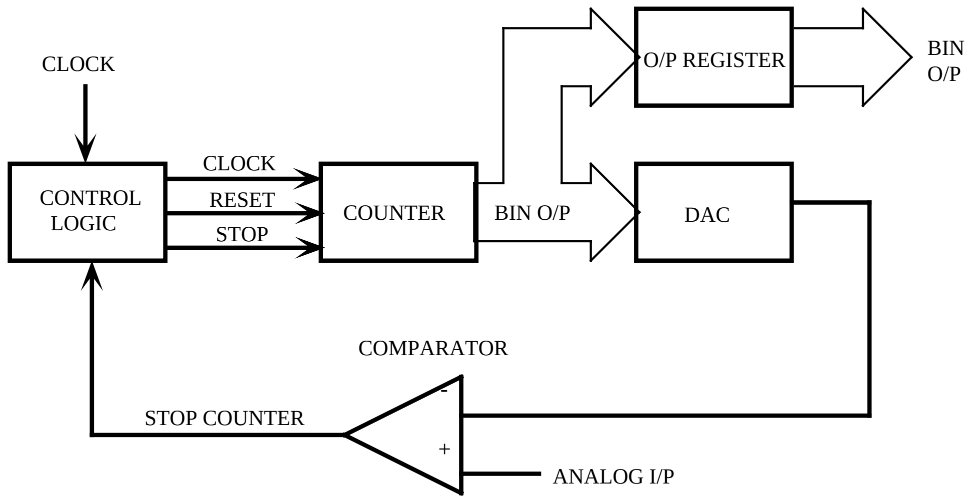
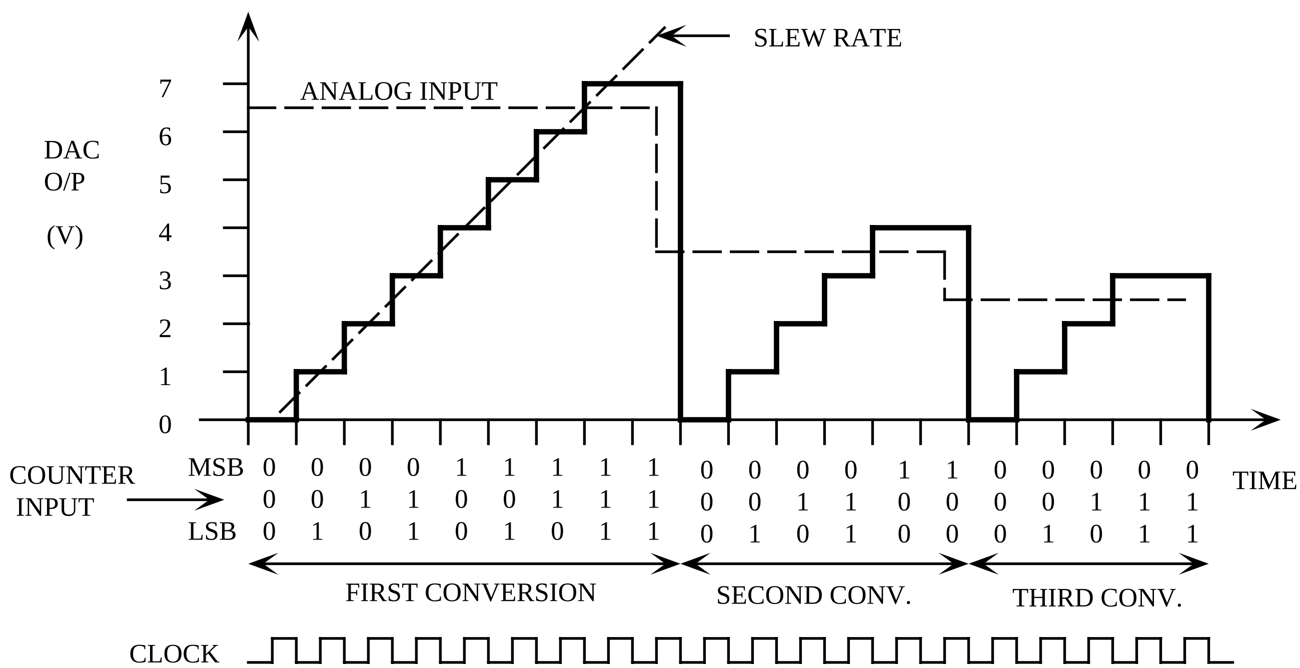
ANALOG TO DIGITAL CONVERTERS .

SYSTEM BLOCK DIAGRAM



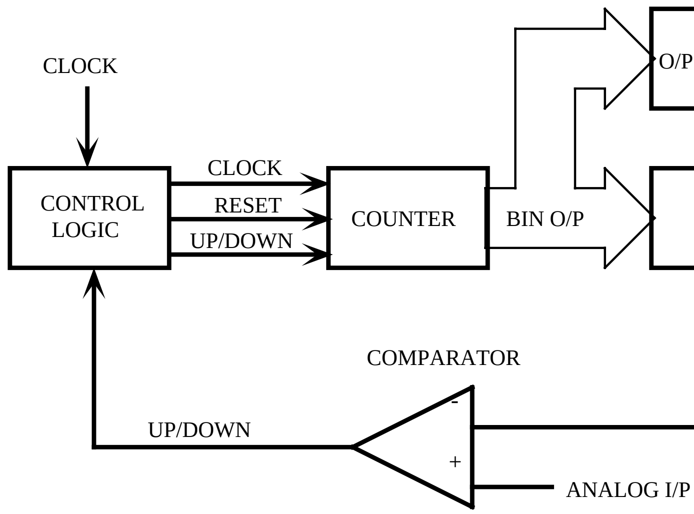
COUNTER ADC

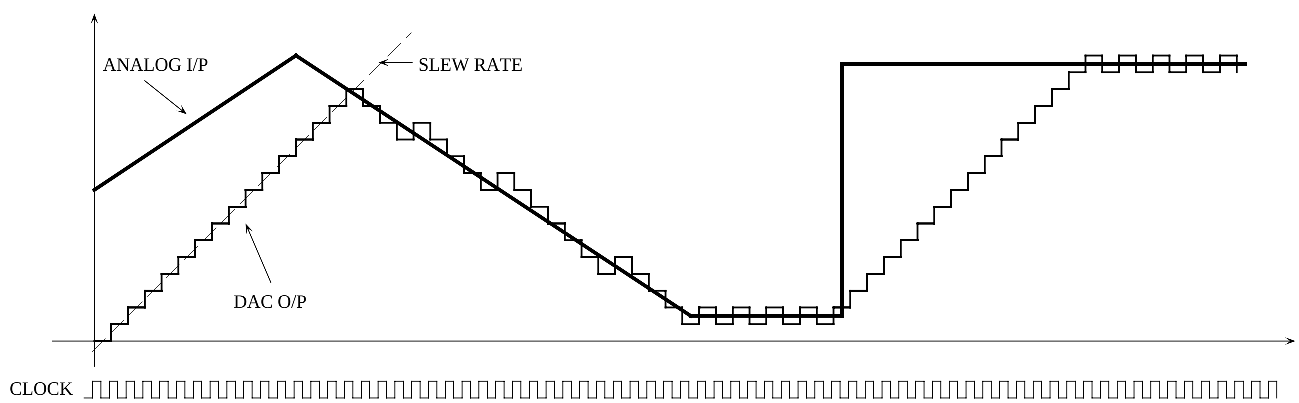




The conversion time of the counter ADC is variable : t_{conv} = (1 to (2^N +1))$*T_{clk}$

TRACKING ADC

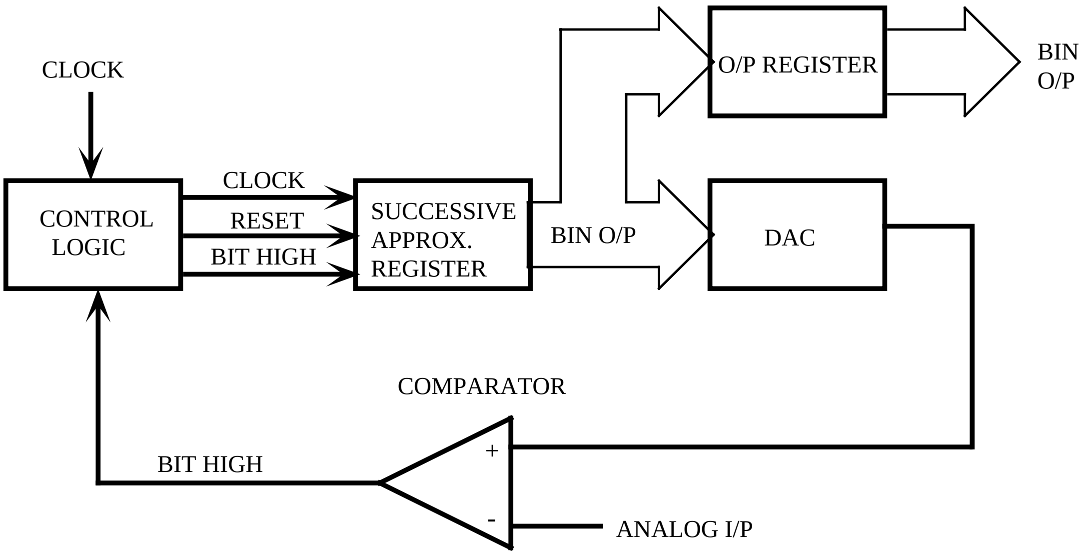




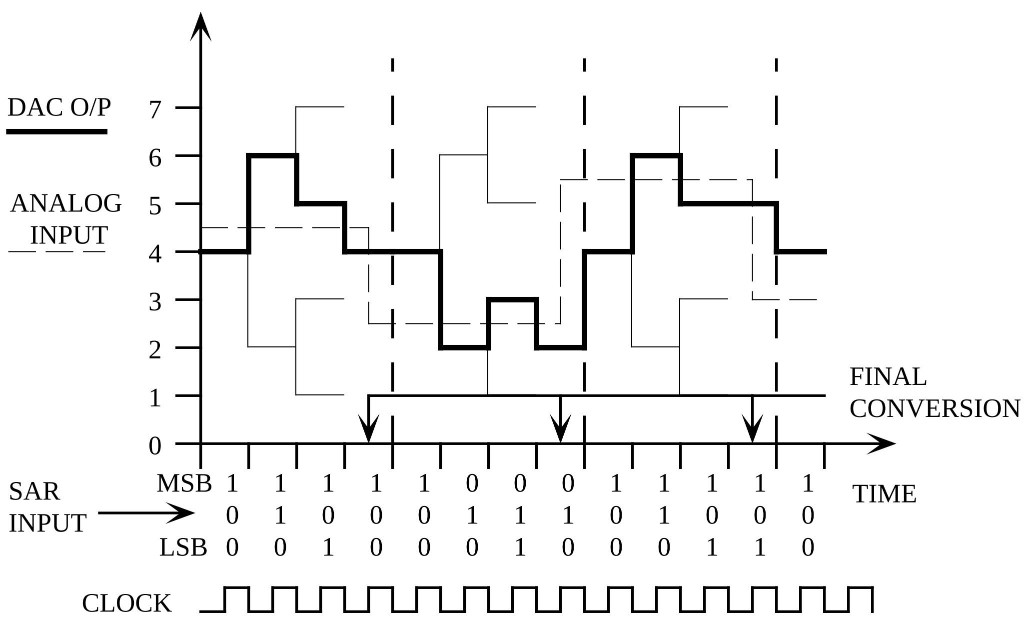
$$slew\ rate\,(SR) = \frac{dV}{dt}\max = \frac{resolution}{T_{clk}} = \Delta V \times F_{clk}$$

For a sinewave, the maximum frequency that can be tracked is $F_{\max} = \dfrac{SR}{2\pi\, V_{peak}}$

SUCCESSIVE APPROXIMATION ADC

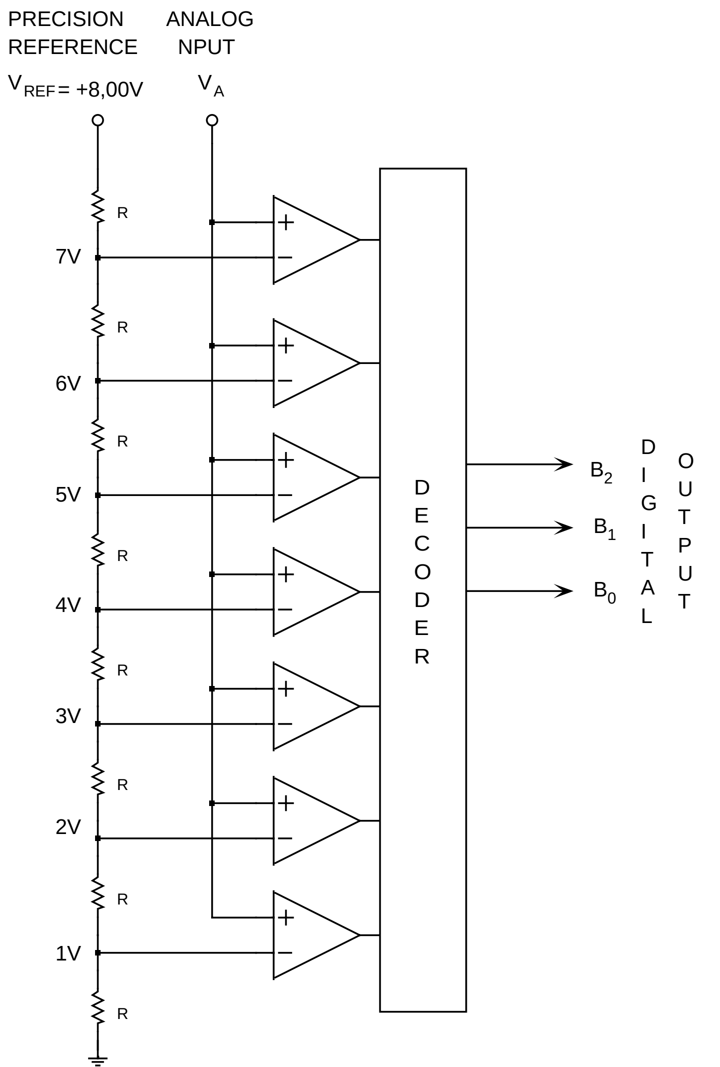


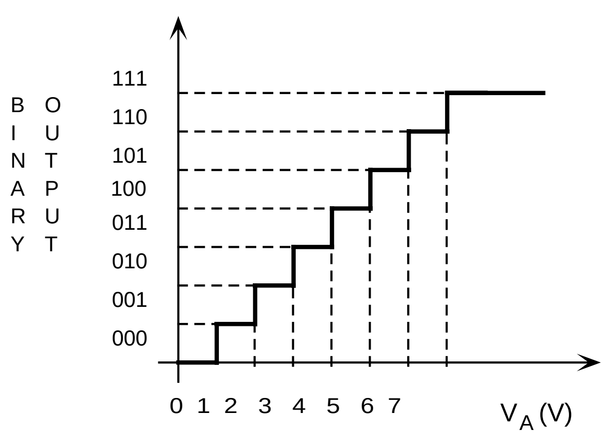
Typical waveforms for three-bit SAR ADC



If $V_{DAC} < V_{AN}$, tested bit remains 1 and if $V_{DAC} > V_{AN}$, tested bit set to 0.
SAR ADC decreases the conversion time to $t_{conv} = (N+1) * T_{clk}$, which is much faster than the counter ADC average conversion time.

FLASH ADC



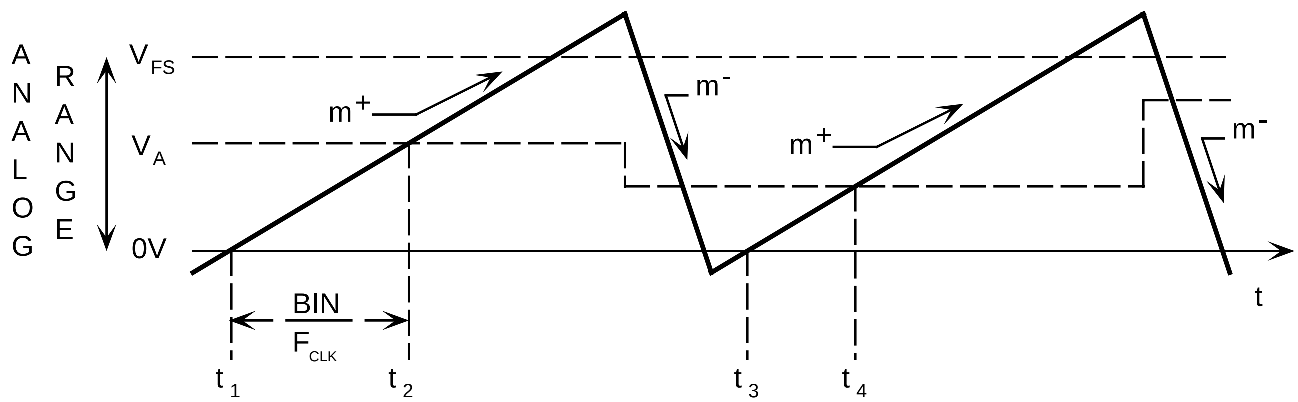


Very fast conversion speed - no counter or clock involved.

For N bits one needs to use $2^N - 1$ comparators and the logic decoder becomes more complex and also raises the conversion time.

Available on a single IC for 6 and 8 bits and possibly more bits in more recent IC's.

SINGLE-SLOPE ADC



t_1: counter starts counting from zero.
t_2: counter is stopped at t_2 when the positive ramp crosses level V_A which is the analog volage being converted. The final count called here BIN is the desired binary conversion which is transferred to an O/P register after the counter has stopped.
Interval t_2-t_3: count is transferred to O/P register, counter is reset to zero and ramp returns to a negative level to initiate the next conversion.

$$m^+ = \frac{\Delta V}{\Delta t} = \frac{V_A - 0}{t_2 - t_1} = \frac{V_A F_{clk}}{BIN} \Rightarrow BIN = \frac{V_A F_{clk}}{m^+}$$

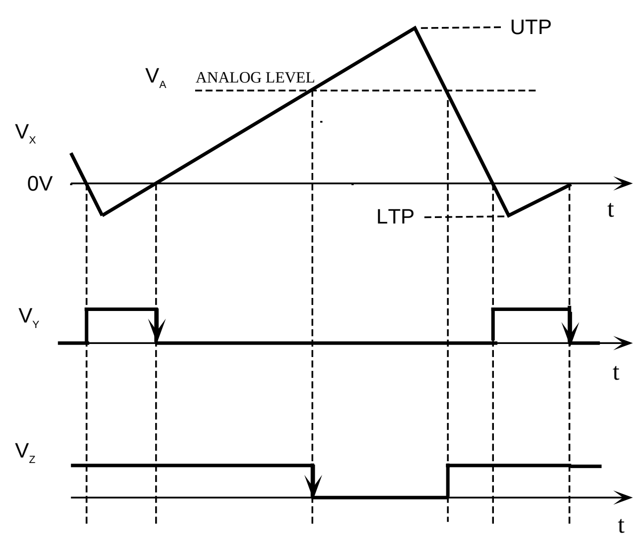
With an N bit counter the analog conversion range is 0V to V_{FS} (full scale voltage) where V_{FS} is given by the following:

$$V_{FS} = V_A \max = \frac{BIN_{max} \times m^+}{F_{clk}} = \frac{(2^N - 1) \times m^+}{F_{clk}} \qquad resolution = \frac{V_A \max - V_A \min}{\#\text{ of steps}} = \frac{V_{FS} - 0}{(2^N - 1)} = \frac{m^+}{F_{clk}}$$

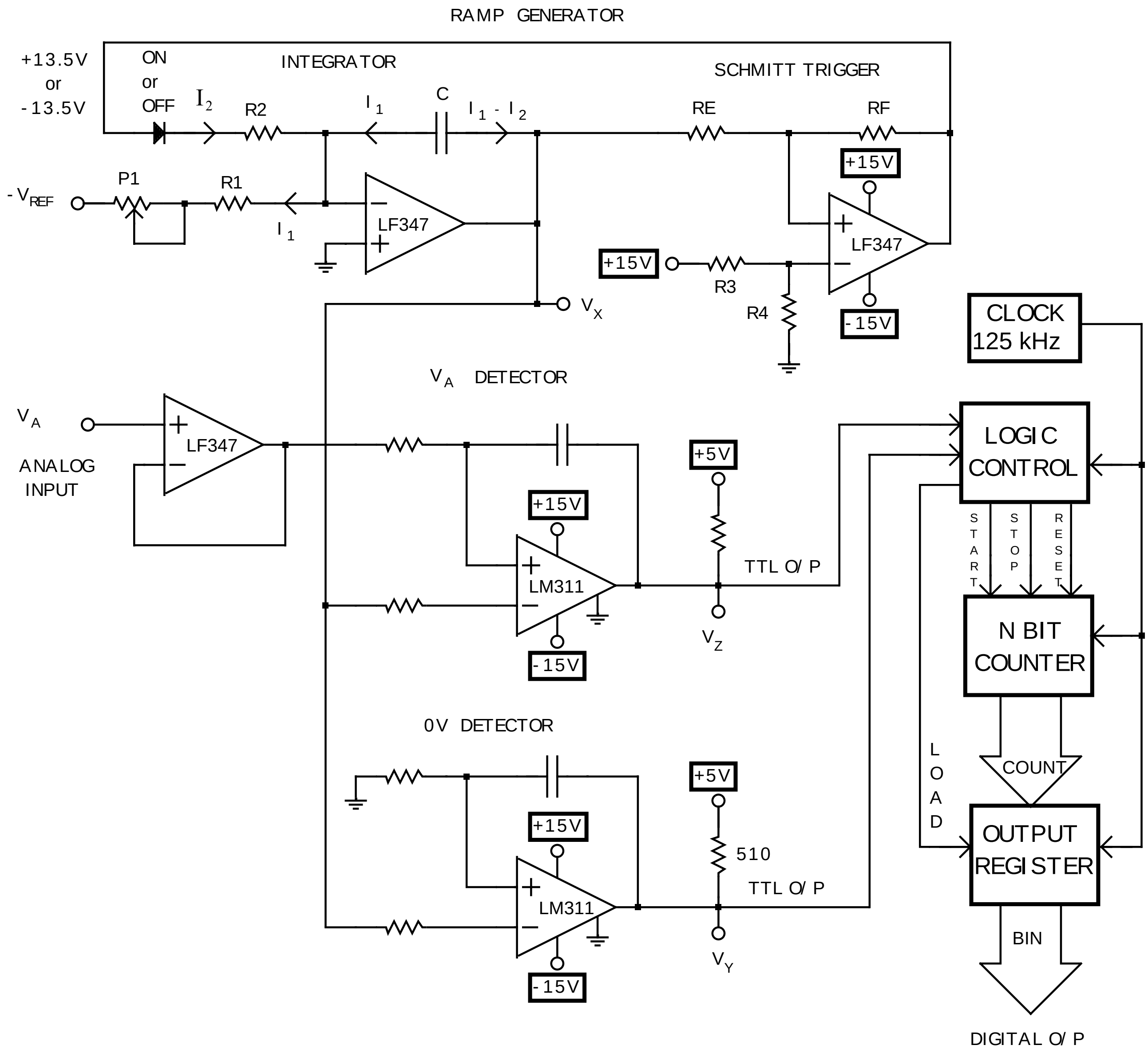
Circuit description
(see next page for circuit)

0V and V_A level detectors tell the logic controller when to start and stop the counter. The ramp signal is implemented using an integrator and a Schmitt trigger which determines the the peak voltages of the ramp signal (V_X) and reverses the direction of the capacitor current: when Scmitt trigger O/P is low, diode is OFF and only I_1 flows through C, and when it is low, diode is ON and net current through C is (I_2-I_1) in opposite direction provided that $I_2 > I_1$.

Circuit waveforms



Circuit diagram



<u>Design example</u>

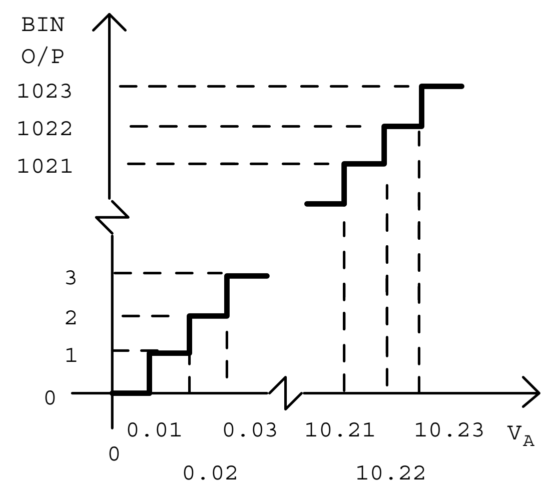
ADC specifications:
- conversion range 0 to 10.23V
- resolution 10 bits
- clock 100 kHz

A) Determine the positive slope required for the ADC and draw the corresponding transfer function.

$$m^+ = \frac{V_A F_{clk}}{BIN} = \frac{V_{FS} F_{clk}}{BIN_{max}} = \frac{10.23 \times 100k}{1023} = 1000\ V/s$$

$$\text{resolution} = \frac{V_A\ max - V_A\ min}{\#\ of\ steps} = \frac{10.23 - 0}{(2^{10} - 1)} = 10\ mV$$

ADC transfer function



B) Determine the integrator components required if $-V_{REF}$ = -10V and $m^- \approx 4\ m^+$ for the ramps. Select currents I_1 and I_2 large enough such that op amp input bias current is negligible and not too large such that op amp O/P is not overloaded.

Let I_1=0.5 mA >> I_{BIAS} , therefore $I_1/C=m^+$ and $C=I_1/m^+$=0.5m/1000=0.5 μF , select <u>0.47 μF</u> standard. $I_1=C\ m^+$ = 0.47μ X 1000 = 0.47 mA.

R1 +P1 = V_{REF}/I_1 = 10/0.47m = 21.28K select <u>R1=20K, 1% (low TC metal film resistor) and P1=2K pot.</u>

$m^- \approx 4\ m^+$ or

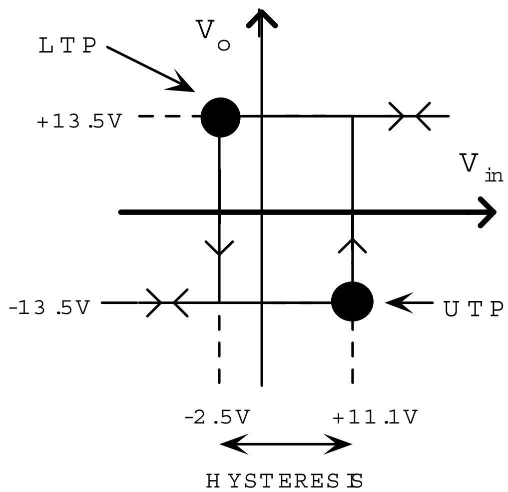
$(I_2 - I_1)/C=4\ I_1/C$ therefore $I_2 = 5\ I_1$ = 5 * 0.47 m = 2.35 mA

R2 = (13.5-0.7)/ 2.35m = 5.44K select <u>5.6K standard</u>

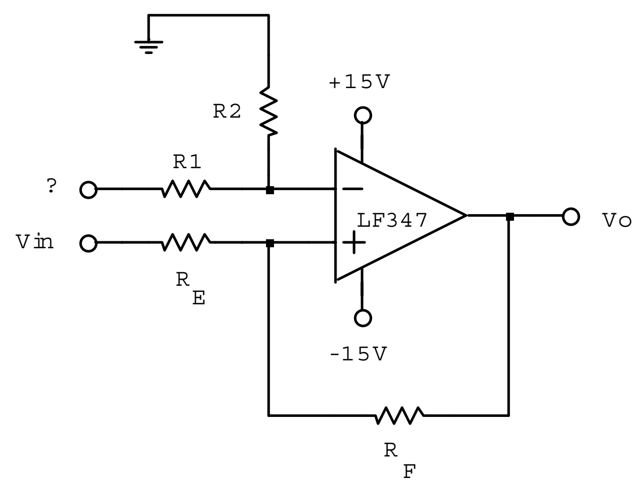
C) Design of the Schmitt trigger

In this application, the trigger points (LTP and UTP) determine the peak voltages of the triangular wave, therefore they must be selected to encompass the analog voltage range of 0 to 10.23V. Arbitarily choose LTP = -2.5V, do not pick LTP too close to 0V and not too far from 0V not to waste time in the negative region. UTP should be selected midway between $V_{SAT}{}^{+}$ min = 12V and V_A max = V_{FS} =10.24V, therefore UTP = (10.24+12)/2 = 11.1V.

Transfer function



Circuit diagram



<u>Design procedure</u>

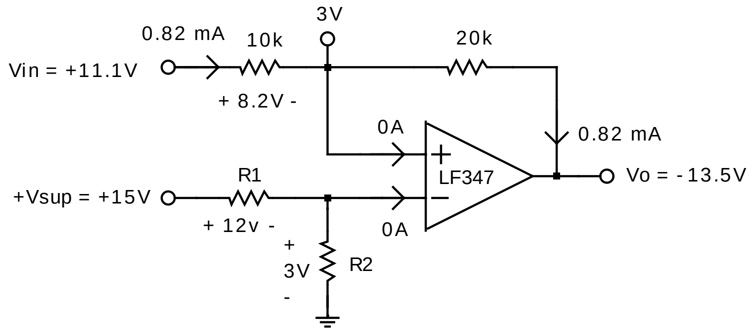
1. Calculate the ratio $\frac{R_F}{R_E} = \frac{V_o^+ - V_o^-}{UTP - LTP}$ and determine standard R_F and R_E values to achieve desired ratio. Select large enough resistors so that op amp O/P is not overloaded - bear in mind that ±13.5V saturation levels are typical for R_L=10k for LF347 and that they will change with R_L seen by op amp O/P.

2. Using standard values of R_E and R_F analyze the circuit in order to find the reference voltage needed by calculating $V^+=V^-$ at one of the trigger points.

3. Calculate standard values of R_1 and R_2 needed for the reference voltage obtained above and to roughly balance the op amp inputs if they are BJT I/P's.

1. $$\frac{R_F}{R_E} = \frac{V_o^+ - V_o^-}{UTP - LTP} = \frac{13.5-(-13.5)}{11.1-(-2.5)} = 1.985 \approx 2$$ let R_F = 20k and R_E = 10k

2. Analyzing the circuit for V_o=-13.5V and V_{in}=UTP, we obtain V_{REF}=V^- =+3V



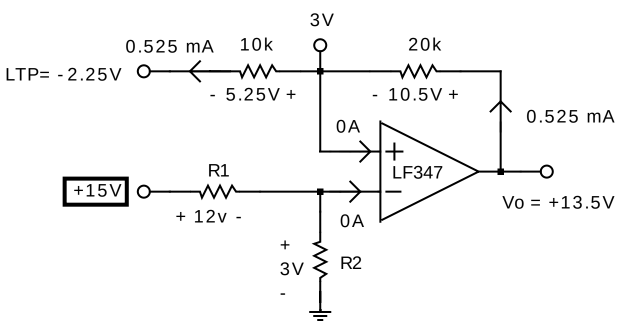
3. $$\frac{V_1}{V_2} = \frac{I_1 R_1}{\underbrace{I_2}_{I_1=I_2} R_2} = \frac{R_1}{R_2}$$

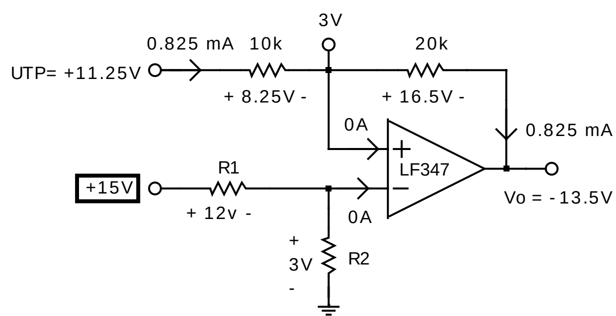
$$\frac{R_1}{R_2} = \frac{12V}{3V} = 4$$

R_1=12K and R_2=3K

We do not have to balance the op amp inputs because of the JFET inputs.

<u>Analysis of actual trigger points</u>

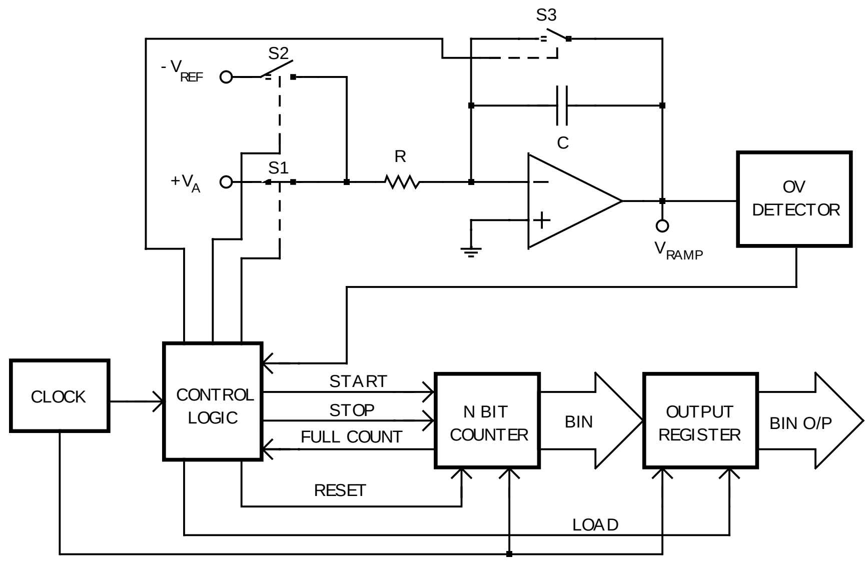




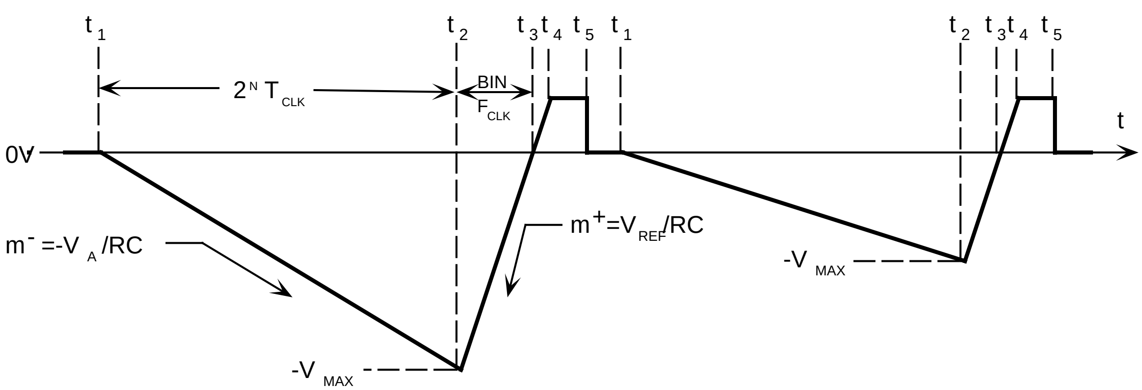
<u>Accuracy of single slope converter</u>

$$BIN = \frac{V_A F_{clk}}{m^+} = \frac{V_A}{V_{REF}} \times F_{clk} RC$$ Since the binary conversion depends on V_{REF}, F_{CLK}, R and C of integrator, this converter is not very accurate. Temperature variations and aging of components will affect values of V_{REF}, F_{CLK}, R and C which will decrease the accuracy. Other factors affecting the accuracy of the converter are the input DC offsets (V_{io}) of the integrator op amp, the 0V detector and the V_A detector. This ADC is less accurate than the dual slope converter.

DUAL-SLOPE ADC



Ramp output (V_{RAMP})



The op amp with R and C form an integrator with the following relationship:

$$V_{RAMP}(t_2) = -V_C = -\frac{1}{C}\int_{t_1}^{t_2} I_C dt + V_{RAMP}(t_1) = -\frac{1}{RC}\int_{t_1}^{t_2} V_A dt + V_{RAMP}(t_1)$$

t_1: V_{RAMP} = 0V, analog voltage $+V_A$ is switched in, counter starts counting from zero and integration starts. $I_C = \frac{V_A}{R} = C\frac{dV_C}{dt}$ Since V_A is a constant voltage, the capacitor will be charged linearly and the slope of V_{RAMP} will be $m^- = \frac{dV_{RAMP}}{dt} = -\frac{V_A}{RC}$.

Interval t_1-t_2: integrator integrates $+V_A$ while counter counts from 0 to 2^N-1 (full count) and resets automatically to 0 at t_2 after 2^N colck pulses. $-V_{REF}$ in switched in on t_2 and $+V_A$ is switched out.

Interval t_2-t_3: integrator integrates $-V_{REF}$ while counter counts from 0 to BIN. BIN is the count when the ramp crosses 0V at t_3 and is also the desired binary conversion.

Interval t_3-t_4: count is loaded in output register and counter is reset to zero for next conversion.

Interval t_4-t_5: $-V_{REF}$ is switched out and V_{RAMP} stays constant (all 3 switches are open, I_C=0A)

Interval t_5-t_1: S3 is closed and C is discharged to 0V for next conversion and then S3 is opened again. At t_1 new V_A is switched in and counter starts counting from zero for next conversion.

$$\left|m^-\right| = \frac{V_A}{RC} = \frac{\Delta V_{RAMP}}{\Delta t} = \frac{V_{MAX}}{2^N T_{CLK}} = \frac{V_{MAX} F_{CLK}}{2^N} \qquad m^+ = \frac{V_{REF}}{RC} = \frac{\Delta V_{RAMP}}{\Delta t} = \frac{V_{MAX}}{BIN \times T_{CLK}} = \frac{V_{MAX} F_{CLK}}{BIN}$$

$$\frac{\left|m^-\right|}{m^+} = \frac{V_A}{V_{REF}} = \frac{BIN}{2^N} \quad \Rightarrow \quad BIN = \frac{V_A}{V_{REF}} \times 2^N$$

ADC resolution: V_{REF} / (2^N)
Conversion range: 0V to $V_A$max or 0V to V_{REF} ((2^N-1) / 2^N)

Design example

A dual slope ADC has the following specifications:-V_{REF}=-4.096V, F_{CLK}=1 MHz and12 bit resolution.

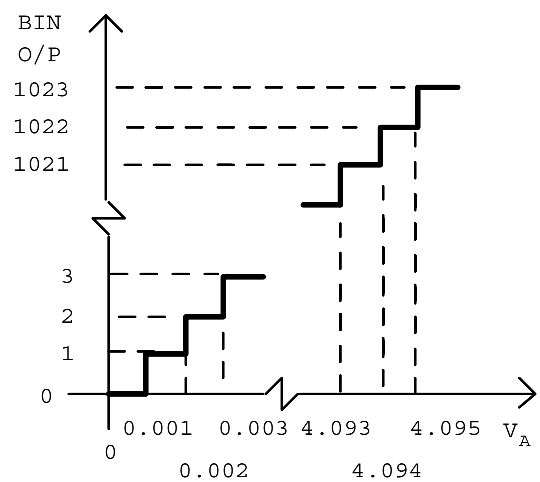
A) Calculate the conversion range of the ADC, its resolution in mV and the binary conversion if V_A = +2V. Also draw its transfer function.

Resolution:
step size $\Delta V = V_{REF} / 2^N = 4.096 / 2^{12} = 1$ mV

Conversion range:
0V to 4.096 ((2^{12}-1) / 2^{12}) = 0V to 4.095V

$$BIN = \frac{V_A}{V_{REF}} 2^N = \frac{2}{4.096} \times 2^{12} = 2000$$

ADC Transfer Function



B) Assuming that V_{sat}=±12V min for integrator op amp, calculate R and C values required for -V_{MAX} ≈ -10V maximum which occurs when V_A is maximum. Value of -V_{max} does not affect conversion but if -V_{MAX} is too small, the ramp will "scrape" too close to 0V level and accuracy of 0V detector will be impaired resulting in reduced ADC accuracy. Maximizing -V_{MAX} will improve ADC accuracy.

$$\left|m^-\right| = \frac{\Delta V_{RAMP}}{\Delta t} = \frac{V_A \max}{RC} = \frac{V_{MAX} F_{CLK}}{2^N} \quad \Rightarrow \quad RC = \frac{V_A \max}{V_{MAX}} \frac{2^N}{F_{CLK}} \qquad RC = \frac{4.095}{10} \frac{2^{12}}{10^6} = 1.6773 \text{ ms}$$

Let $I_{C\ max}$ ≈ 1 mA = V_{REF} / R = 4.096 / R, therefore R = 4.096K

C = 1.6773m / 4096 = 0.409 µF, select next <u>higher</u> standard value for lower V_{MAX} (do not go too close to V_{SAT} min of op amp) C = 0.47 µF, 2%

R = 1.677m / 0.47µ = 3568.7Ω, that is R = 3.6k,1% (fixed metal film resistor)

Note: RC value is not critical because it does not affect the conversion as long as it is stable during the conversion interval.

$$-V_{MAX} = -\frac{V_A \max 2^N}{RC \times F_{CLK}} = -\frac{4.095 \times 2^{12}}{3.6K \times 0.47\mu \times 10^6} = -9.91V$$

This value is safe because it is far enough from V_{SAT} min = -12V min.

Accuracy of dual slope converter

$BIN = \frac{V_A}{V_{REF}} \times 2^N$ Since the binary conversion is independant of F_{CLK}, R and C of integrator, this converter is much more accurate than the single-slope converter. Temperature variations and aging of components will affect values of R, C and F_{CLK} but conversion will be very accurate as long as V_{REF} has a low temperature coefficient. Other factors affecting the accuracy of the converter are the input DC offsets of the integrator op amp and of the 0V detector.