If the two FET's are not matched, the larger the source resistor is, the less difference there will be between $I_{D1}$ and $I_{D2}$ as can be observed on the graph shown beside. Line A-B is the bias line for circuit-3 and line C-D is the bias line for circuit-4.

**Example: bias line A-B**

$V_R = 4.7 + 0.7 = 5.4 \text{ V avg}$

Point A

$V_{GS} = -4 \text{ V}$, $I_D = \frac{(V_R-V_{SG})}{R_{SC}}$

$I_D = \frac{(5.4-4)}{0.14} = 10 \text{ A}$

Point B

$V_{GS} = -5 \text{ V}$, $I_D = \frac{(V_R-V_{SG})}{R_{SC}}$

$I_D = \frac{(5.4-5)}{0.14} = 2.86 \text{ A}$

For line C-D, $V_R = 4.7 + 1.4 = 6.1 \text{ V}$

The maximum load current will be:

$I_{MAX} = I_{MAX(REG)} + 2 I_{MAX(Q)}$

$I_{MAX} = 1 \text{ A} + 2 \times 0.7/0.14 = 11 \text{ A}$

$I_{C3\text{max}} = I_{in}(V_{GS}+V_{BE})/R = I_{C3\text{max}} = 1-(4.7+0.7)/18 = 0.7 \text{ A}$

Here there is no DC gate current therefore $I_{MAX}$ will vary only due to variations of $V_{BE3}$. $R$ is made higher here in order to keep its maximum power rating down because the voltage is substantially higher then what it was for BJT's.

$V_{R_{max}} = V_{BE3}+V_{GS_{max}} = 0.7 + 4.7 = 5.4 \text{ V}$

$I_{R_{max}} = 5.4/18 = 0.33 \text{ A} < I_{REG_{max}} \text{ OK}$

$P_{R_{max}} = 5.4^2/18 = 1.62 \text{ W} \text{ (use 5W rating)}$

The maximum load current will be:

$I_{MAX} = I_{MAX(REG)} + 2 I_{MAX(Q)}$

$I_{MAX} = 1 \text{ A} + 2 \times 1.4/0.28 = 11 \text{ A}$

$I_{C3\text{max}} = I_{in}(V_{GS}+V_{BE})/R = I_{C3\text{max}} = 1-(4.7+1.4)/18 = 0.66 \text{ A}$

Here there is no DC gate current therefore $I_{MAX}$ will vary only due to variations of $V_{DF}$ and $V_{BE3}$. $R$ is made higher here in order to keep its maximum power rating down because the voltage is substantially higher then what it was for BJT's.

$V_{R_{max}} = V_{BE3}+V_{GS_{max}} = 1.4 + 4.7 = 6.1 \text{ V}$

$I_{R_{max}} = 6.1/18 = 0.339 \text{ A} < I_{REG_{max}} \text{ OK}$

$P_{R_{max}} = 6.1^2/18 = 2.07 \text{ W} \text{ (use 5W rating)}$