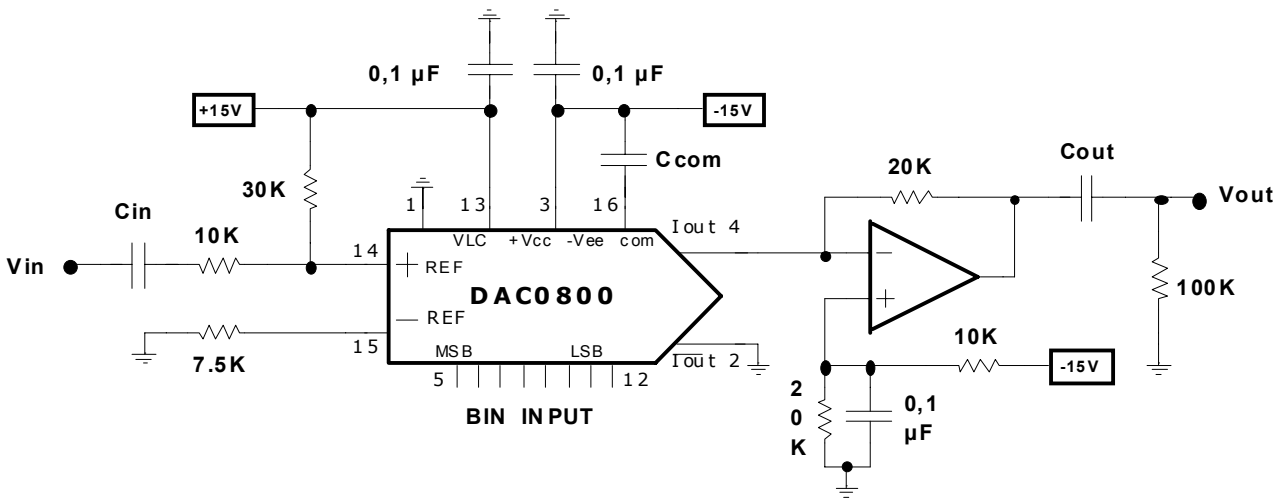


**DIGITAL TO ANALOG CONVERTERS**

NO.1 Design a DAC that provides a -5,12V to +5,12V-LSB using a DAC-08: assume TTL inputs.

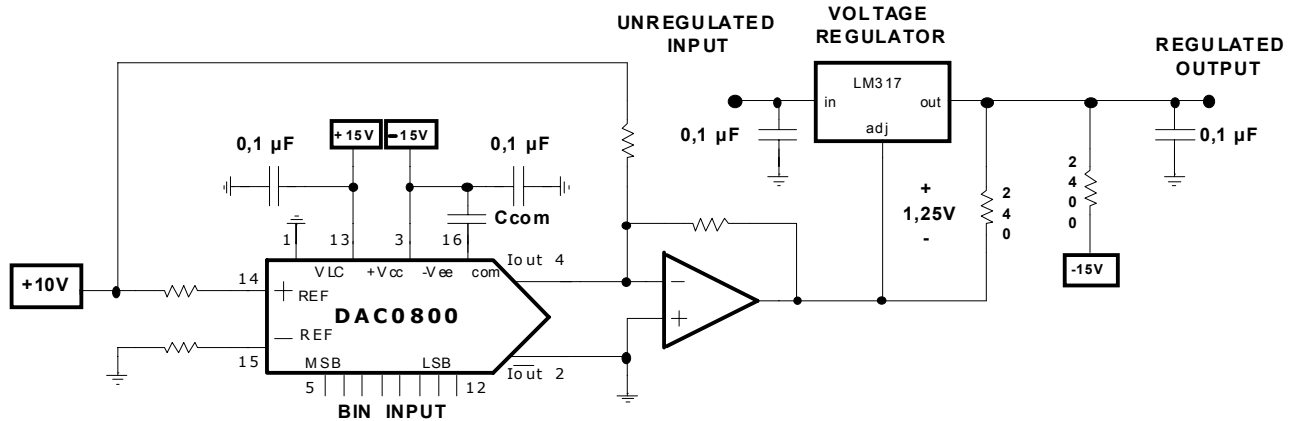
NO.2 Design an amplifier/attenuator with digital gain control using a DAC1220. The gain should range from 0 to 20v/v. Use LF347 op amps and maximise the bandwidth. Also make the input resistance very large ( $R_{in} > 10\text{ M}\Omega$ ).

NO.3



- A) Determine the DC voltage range at the op amp output.
- B) Determine the maximum AC input amplitude that will either clip the output or clip the reference current, whichever comes first. Explain why reference current cannot go negative.
- C) Determine the minimum values of  $C_{in}$  and  $C_{out}$  if the frequency of  $V_{in}$  spans a range of 50 Hz to 10 kHz. Also determine an appropriate  $C_{com}$  value and explain its function.
- D) Determine the AC gain of the circuit as a function of the binary input and plot the gain-BIN characteristic showing all relevant values.
- E) If  $V_{in} = 1.2\text{V}$  and  $\text{BIN} = 124$ , what is  $V_{out}$ ?

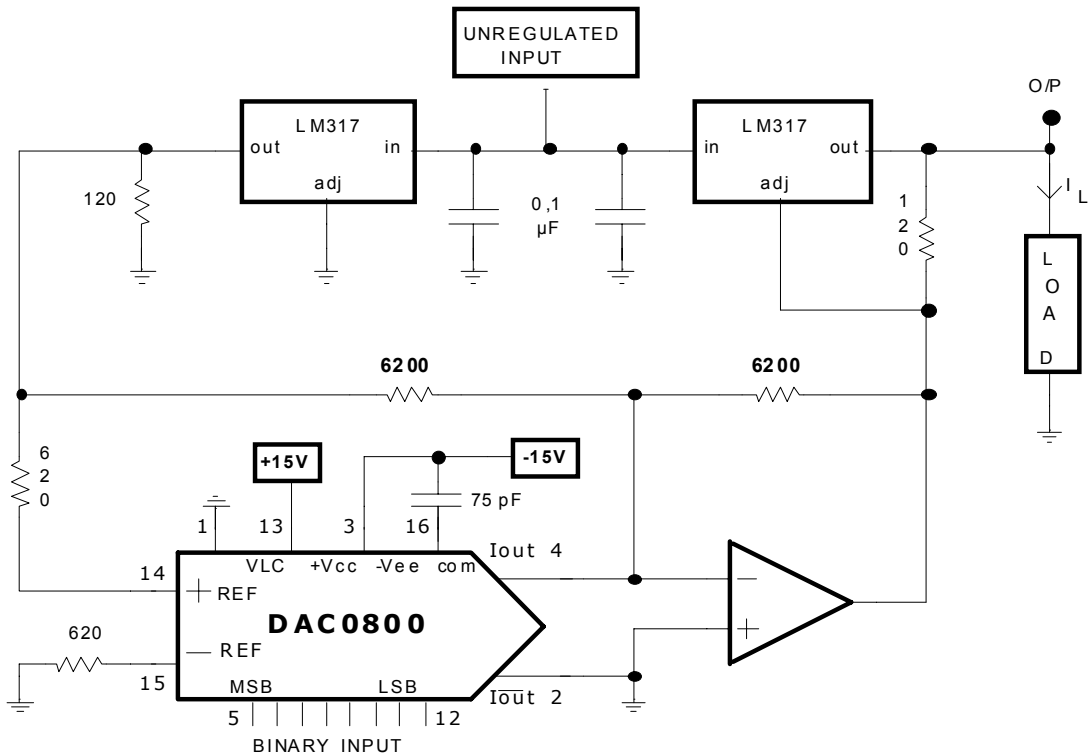
No.4 PROGRAMMABLE DC POWER SUPPLY



NOTE: the 1,25V drop across the 240 resistor is the internal voltage reference of the LM317 regulator that appears across the regulator output pin and the adjustment pin. The +10V at the DAC input should be a precision reference voltage. The minimum load current needed to guarantee operation of the LM317 is specified as 10 mA worst case.

- A) Design the circuit for +0,25V to 19,375V range
- B) Draw the transfer characteristic showing all relevant parameters.

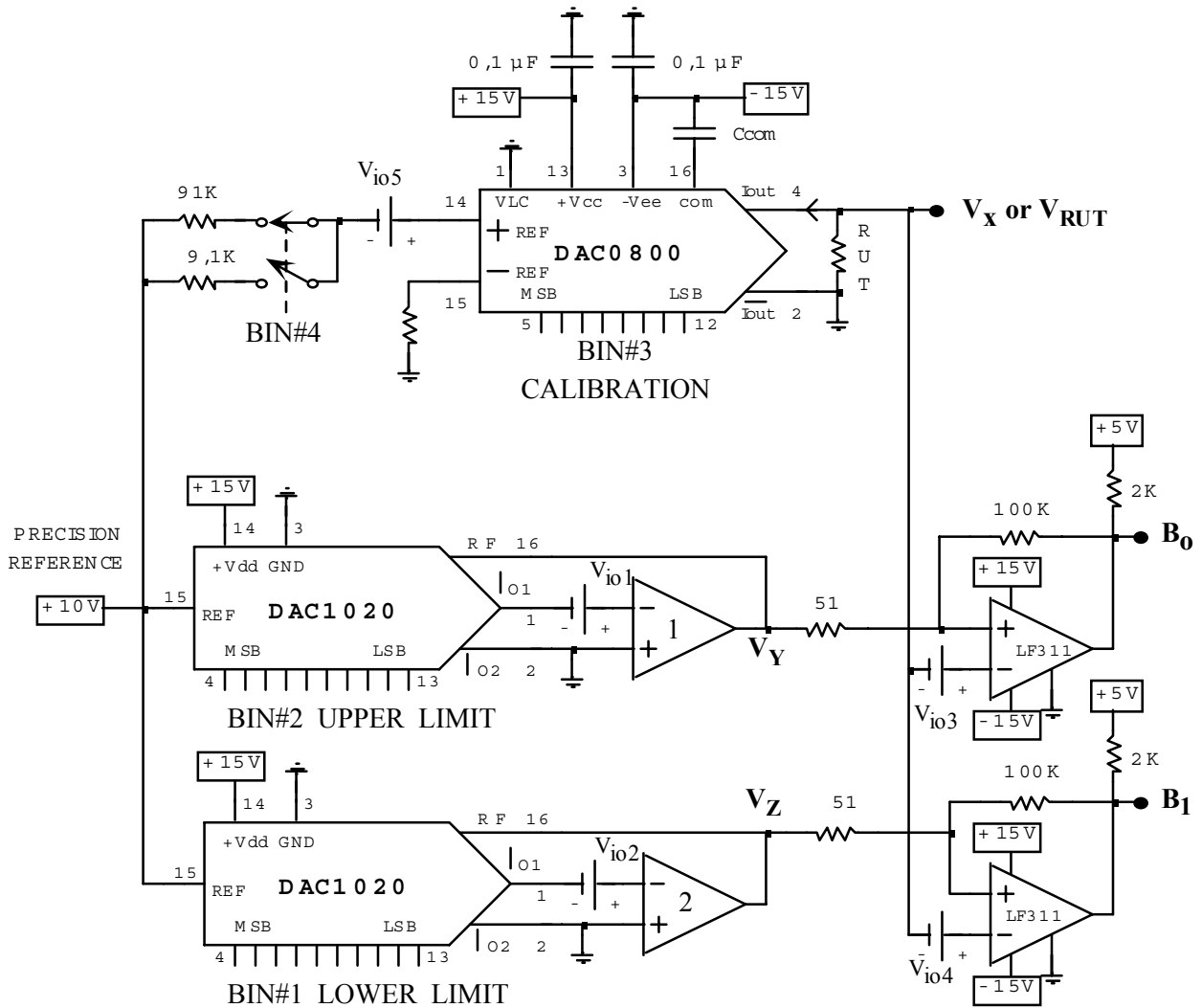
No.5 PROGRAMMABLE DC POWER SUPPLY



No 5 A) Determine the output voltage range and the resolution of  $V_O$ .

- B) Which resistor should we trim in order to null the output when it should be zero? Explain.
- C) Modify the circuit in order to obtain a minimum O/P of +1V and a resolution of 20 mV.
- D) Determine the maximum op amp O/P current. Modify the circuit to reduce this maximum current to 5 mA and still guarantee a minimum load current of 11 mA for the LM317.

No.6 RESISTOR TOLERANCE TEST CIRCUIT



RUT: resistor under test      LF311 outputs: 0V and +5V

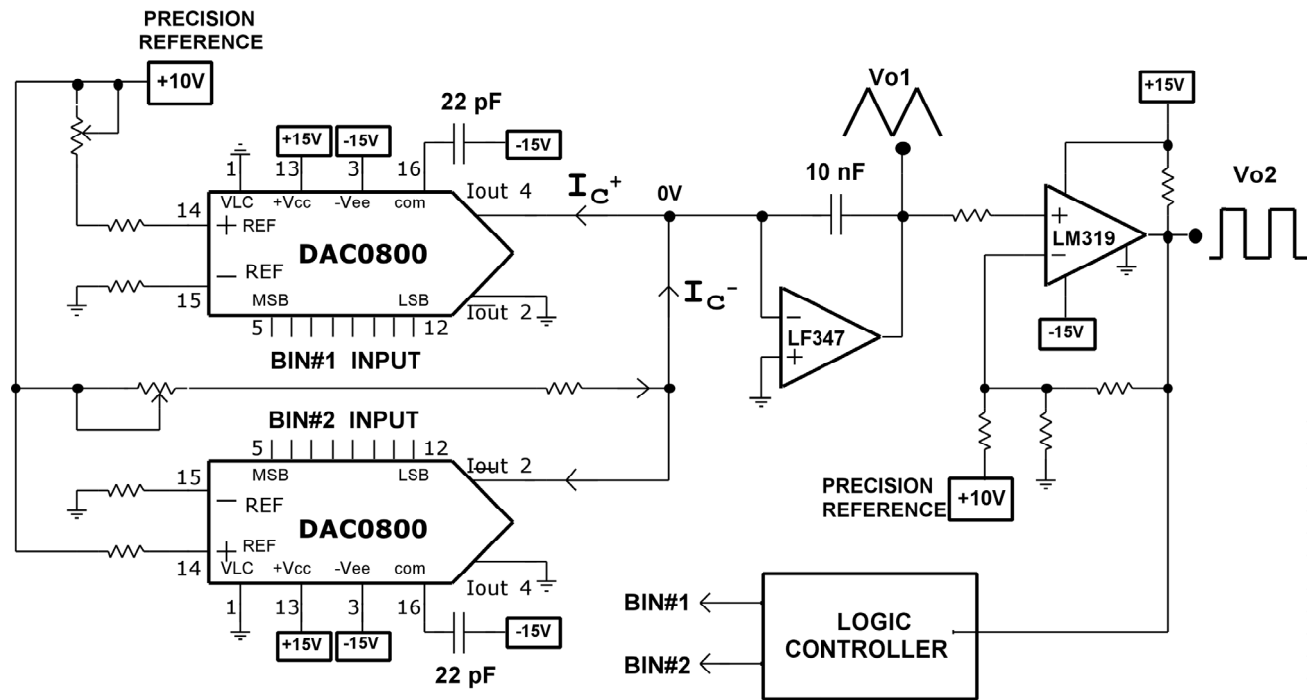
The above circuit is used for automated testing of resistors. BIN#4 selects the the 9.1K resistor for the 0 to 10K range and the 91K resistor for the 0 to 100K range. BIN#3 is used to calibrate  $V_{out}$  of the DAC-0800 to exactly -9.00V with  $R_{UT}=10K$  or  $100K$  for the 0-10K or 0-100K ranges respectively using a calibration  $R_{UT}$ . The two LF311's form a window comparator used to pass or reject the resistor if tolerance is not met.

- A) Determine the typical calibration value of BIN#3.
- B) Assuming we are testing 2% resistors, determine the resistance versus BIN#1 and BIN#2 characteristics for the two ranges and label with all relevant parameters. What is the minimum resistance step that can be resolved in each range?
- C) The LF311 have a maximum  $V_{io}$  of  $\pm 4$  mV at 25 °C and let us assume that the op amps have the same maximum  $V_{io}$ . The cumulative error on the LF311 detection levels will be:  

$$\Delta V_{det} = \pm V_{io} (\text{comp}) \pm V_{io} (\text{op amp}) + \text{hysteresis}$$

What is  $\Delta V_{det}$  maximum and what % error does it represent resistance wise?  
 What is the minimum % tolerance test that can be achieved given the above answer?

No.7 PROGRAMMABLE PW and SW FUNCTION GENERATOR



- A) Design the Schmitt trigger for  $\pm 7.5$ V trigger points.
  - B) Design the DAC circuits to provide a PW and SW range (square wave output) of 100  $\mu$ s to  $\infty$  for BIN#x = 0 to 255.
  - C) If the LF347 have a minimum slew rate of 7 V/ $\mu$ s, is the o amp fast enough to handle the triangular wave output?
- NOTE: The logic controller switches BIN#1 and BIN#2 to proper values to obtain the desired PW and SW at  $V_{o2}$ .  $I_{C^+}$  should be zero when  $I_{C^-}$  is activated and vice-versa.
- D) Draw the PW and SW (versus BIN#x) characteristic showing relevant figures.

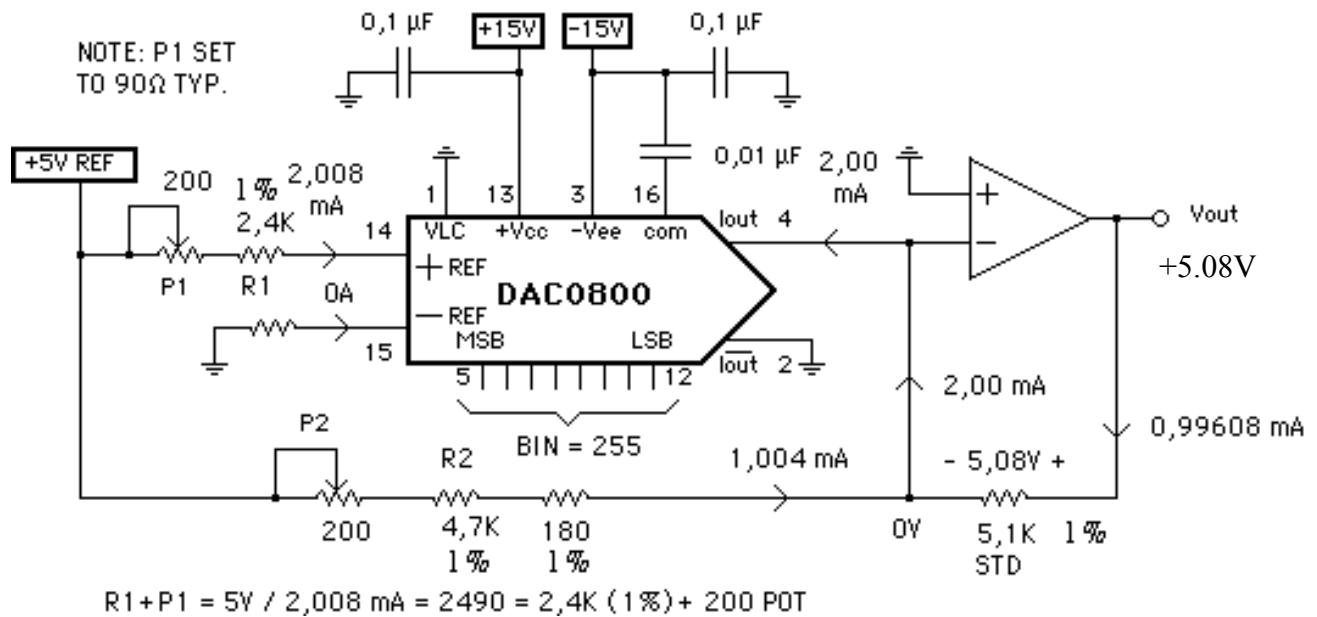
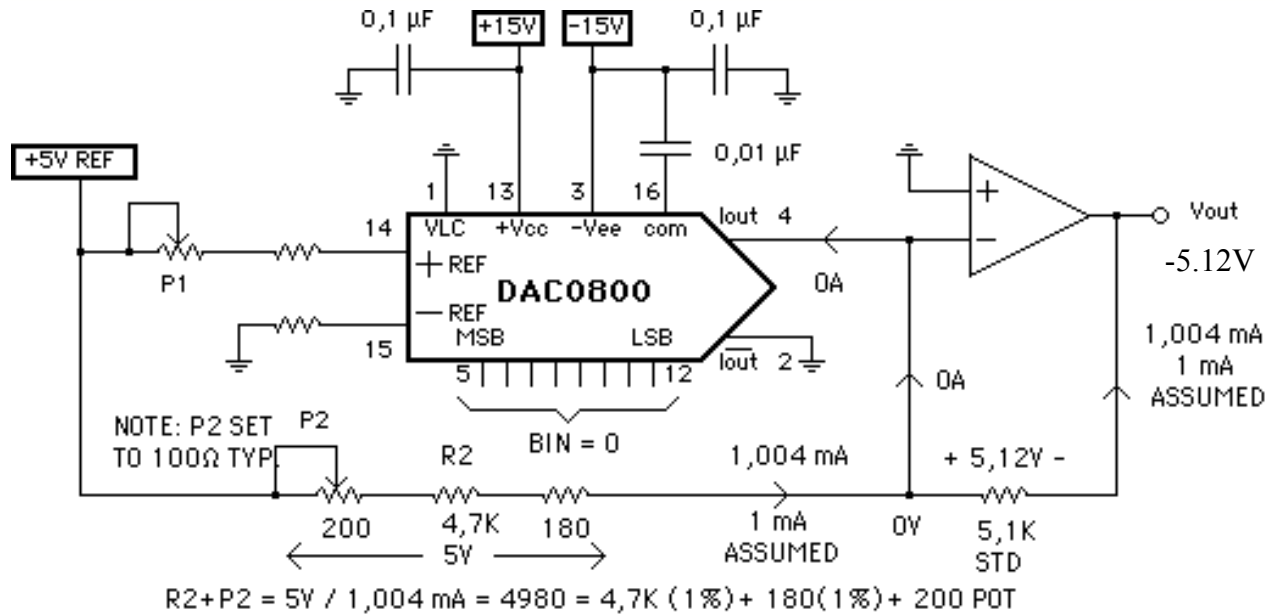


**SOLUTIONS**

No.1

$$V_o = 5,12V \text{ to } +5,12V - \Delta V_o \Rightarrow 5,12V - \Delta V_o - (-5,12) = 255\Delta V_o \Rightarrow \Delta V_o = 40mV$$

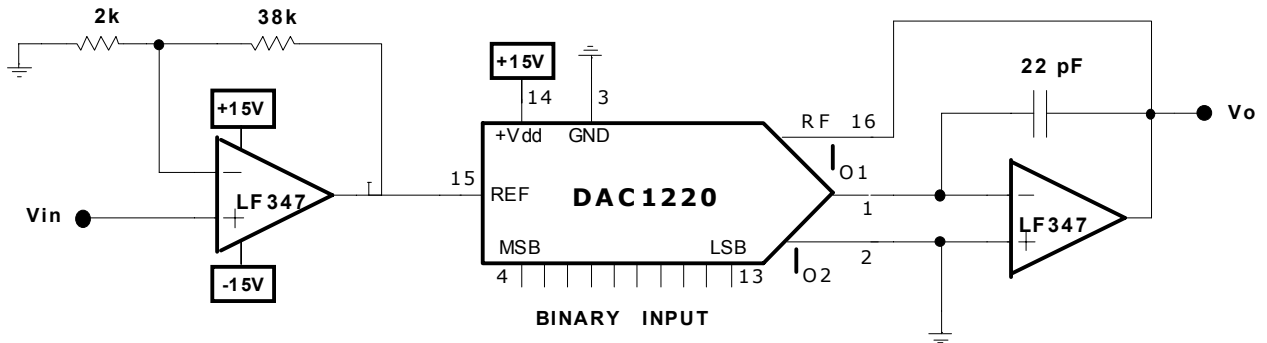
$V_o = -5,12V \text{ to } +5,08V$  in 40 mV increments.



Calculation of  $I_{REF}$  :

$$I_o = I_{REF} \times \frac{255}{256} = 2,00 \text{ mA} \Rightarrow I_{REF} = 2,004 \text{ mA}$$

No.2



The DAC provides a gain of 0 to  $-(4095/4096)$  and the first stage is a non-inverting amplifier with a gain of 20 V/V. Therefore the overall gain is:  $V_o = -\frac{BIN}{2^{12}} \times 20 \times V_{in}$

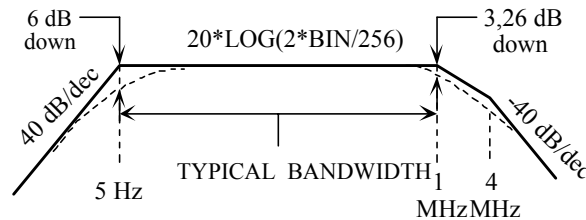
The input resistance of the DAC-1220 varies anywhere from 10K to 20K - see data sheets. The input amplifier/buffer will prevent loading of the signal source.

The typical GBW of the LF347 is 4 MHz, therefore the input amplifier has a  $BW = \beta_v \text{ GBW} = 0,19 \text{ MHz}$ . Using a 22 pF compensation cap for the second LF347, the typical cutoff frequency is about 0,5 MHz according to the DAC1220 datasheets (see figure 3 of data sheets). Therefore the overall cutoff frequency or bandwidth will be about 0,19 MHz.

No.3 A)  $V_{OPA(out)} = -10V$  to  $-39 \text{ mV}$  for  $BIN = 0$  to 255

B)  $V_{SAT} = \pm 12V$  min for LF347 at  $R_L = 10K$ , therefore  $I_{out(AC)} = 12V_P/20K = 0,6 \text{ mA}_P$  max for  $BIN = 255$  and  $I_{REF(AC)} = 0,6m \cdot 256/255 = 0,602 \text{ mA}_x$  which is impossible because  $I_{REF(DC)} = 0,5 \text{ mA}$ , therefore  $I_{REF(AC)} = 0,5 \text{ mA}_P$  max which corresponds to  $V_{in} = 0,5 \text{ mA}_P \cdot 10K = 5V_P$ .

C) In order to not attenuate signals at 50 Hz, let  $F_{LO} = 5 \text{ Hz} = (2\pi \cdot 10K \cdot C_{in})^{-1} = (2\pi \cdot 100K \cdot C_{out})^{-1}$ , therefore  $C_{in} = 3,3 \mu F$  and  $C_{out} = 0,33 \mu F$ .



$C_{com} = 15 \text{ pF}$  is given in datasheets for 1 MHz BW of DAC-0800 - if  $C_{com}$  is increased, BW of DAC0800 will decrease. LF347 has  $\beta_v = 1$  because DAC0800 output is a current output with high resistance, therefore  $BW = \text{GBW}$  of op amp.

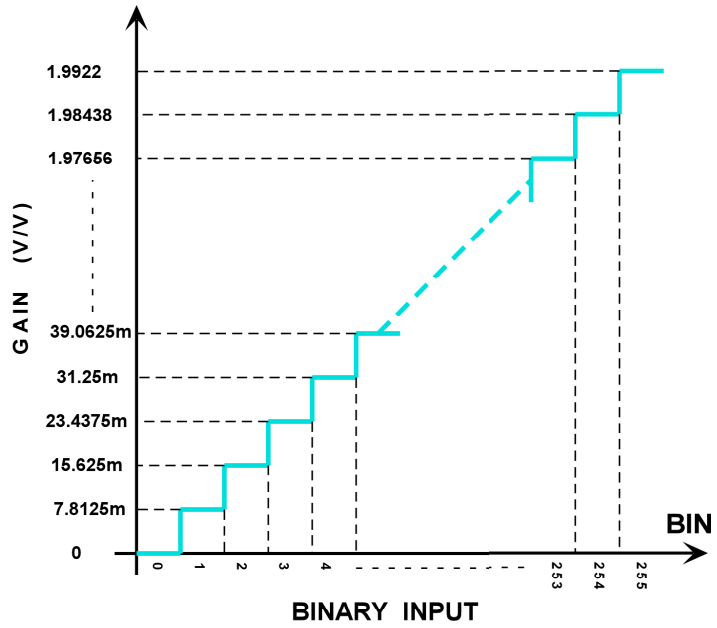
D)

$$A_v = 2 \times \frac{BIN}{2^8}$$

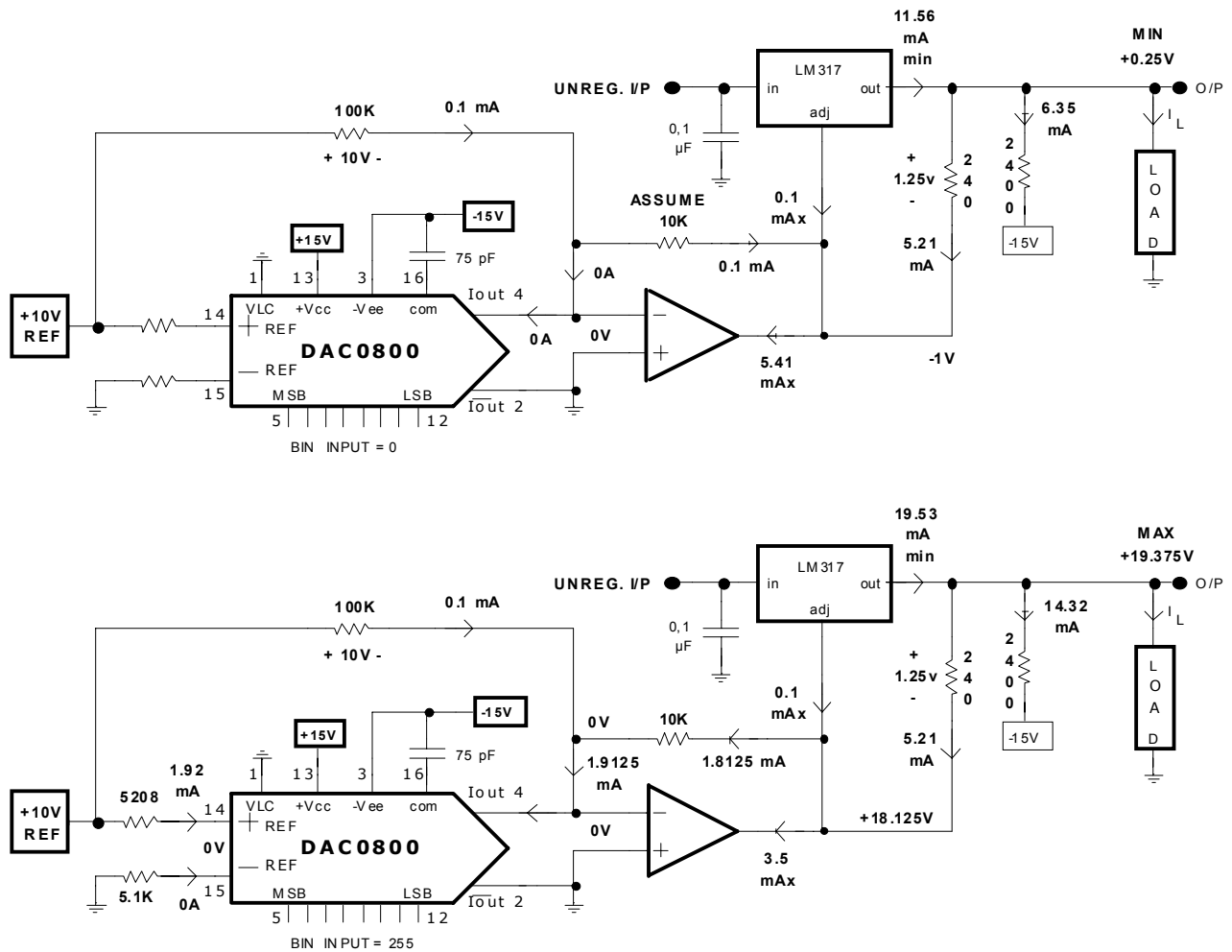
$$\Delta A_v = 2/256$$

$$\Delta A_v = 7.8125mV/V$$

E)  $V_{out} = 1,1625V$



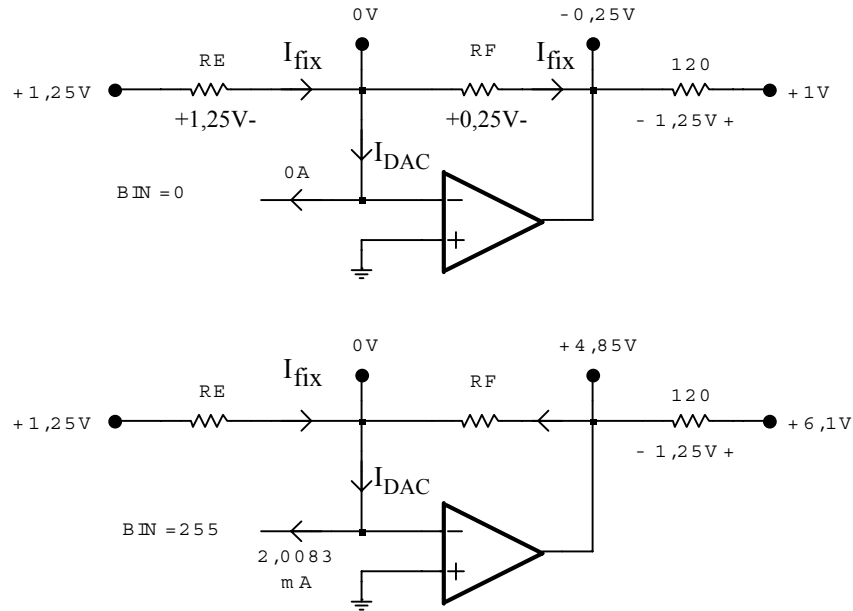
No.4



No.5 A)  $V_O = 0$  to  $+12,45V$   $\Delta V_O = 48,83$  mV

B) On your own!

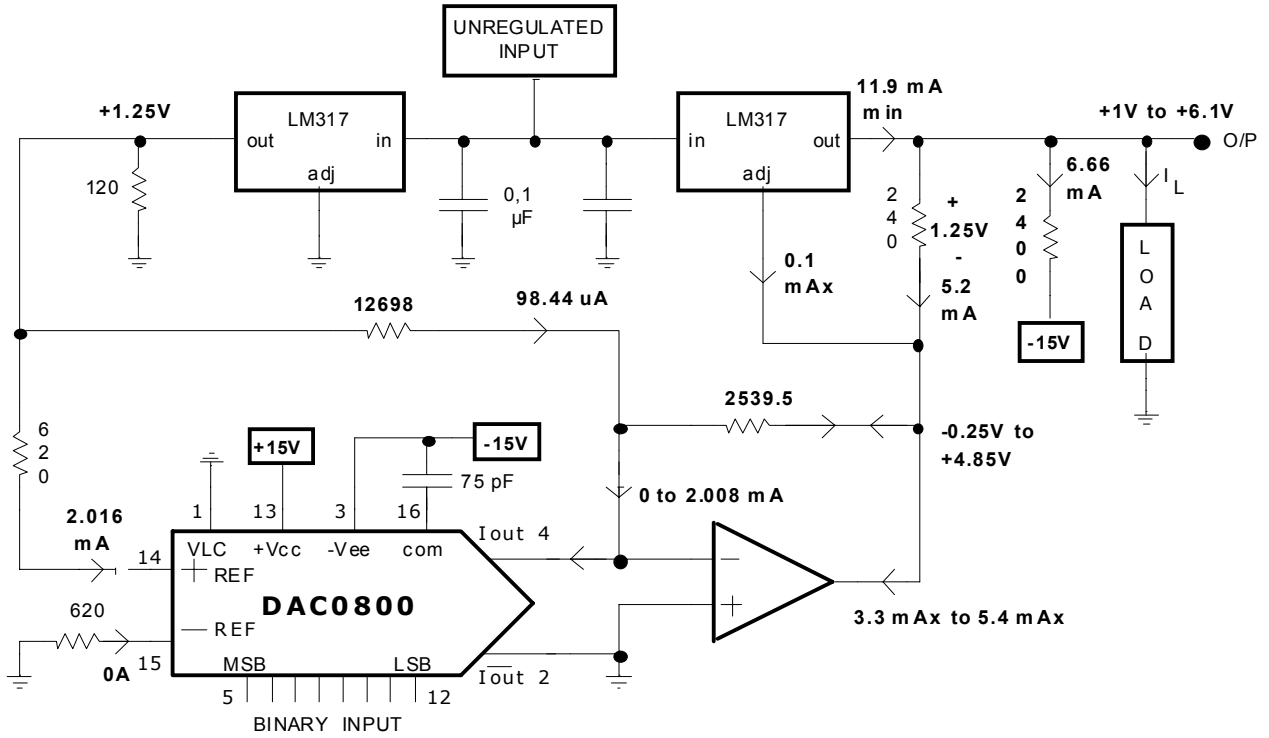
C)  $V_O \text{ min} = +1V$   $V_O \text{ max} = 1V + 20$  mV \* 255 = 6,1V



From the above circuit, we have

$$\frac{I_{FIX} R_F}{I_{FIX} R_E} = \frac{0,25}{1,25} = \frac{R_F}{R_E} = 0,2 \quad \text{and} \quad 4,85V = \left( 2,0083m - \frac{1,25}{R_E} \right) R_F = \left( 2,0083m \times R_F - 1,25 \frac{R_F}{R_E} \right)$$

$$4,85V = (2,0083m \times R_F - 1,25 \times 0,2) \Rightarrow R_F = 2359,5 \quad \text{and} \quad R_E = 5 \times 2359,5 = 12698$$



D) Look at above circuit.

No.6 A)

$$V_{RUT} = -I_{REF} \frac{BIN_3}{256} \times R_{UT}$$

$$BIN_3 = \frac{-V_{RUT} \times 256}{I_{REF} \times R_{UT}}$$

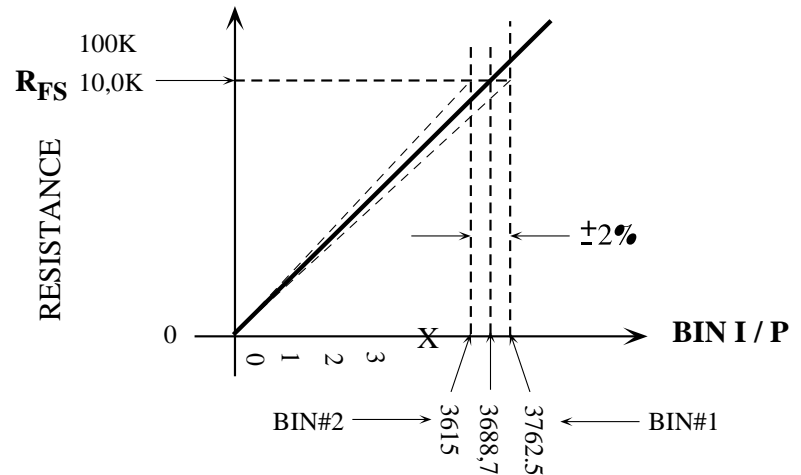
$$BIN_3 = \frac{9 \times 256}{(10 / 9,1K) \times 10K} = 209,66$$

$BIN_3 = 210$  typical, same for all ranges.

$$\Delta R_1 = 10K / 3688,7 = 2,711\Omega$$

$$\Delta R_2 = 100K / 3688,7 = 27,11\Omega$$

B) TRANSFER CHARACTERISTIC



$$V_{RUT} \pm V_{io3} = V_Y \times \frac{100K}{51+100K} + V_{B_0} \times \frac{51}{51+100K} = \frac{V_Y}{1.00051} + \frac{0 \text{ or } 5}{1962}$$

$$V_{RUT} \pm V_{io3} = \frac{V_Y}{1.00051} + (0 \text{ or } 2.55mV) \Rightarrow V_Y = 1.00051(V_{RUT} \pm V_{io3}) - 1.00051(0 \text{ or } 2.55mV)$$

$$V_Y = -10 \times \frac{BIN_1}{2^{12}} \pm V_{ool} \approx 1.00051 \times V_{RUT} \pm V_{io3} - (0 \text{ or } 2.55mV)$$

$$BIN_1 = \frac{1.00051 \times V_{RUT} \pm V_{io3} \pm V_{ool} - (0 \text{ or } 2.55mV)}{-10} \times 2^{12}$$

$$BIN_1 = \frac{1.00051 \times (0 \text{ to } -9.00V) \pm 4mV \pm 4mV - (0 \text{ or } 2.55mV)}{-10} \times 2^{12}$$

$$BIN_1 = \frac{(0 \text{ to } -9.00459V) + (5,45mV \text{ to } -10,55mV)}{-10} \times 2^{12}$$

$$BIN_1 = (-2.23 \text{ min, } 0.5 \text{ ideal, } 4,32 \text{ max}) \text{ to } (3686.05 \text{ min, } 3688.7 \text{ ideal, } 3692.6 \text{ max})$$

$$\%error = \frac{\Delta R_{UT}}{R_{UT}} \times 100 = \frac{(-2.23 \text{ min or } +4,32 \text{ max})}{BIN_1} \times 100$$

$$\%error = \frac{\Delta R_{UT}}{0,1 R_{FS} \rightarrow R_{FS}} \times 100 = \frac{(-2.23 \text{ min or } +4,32 \text{ max})}{368.82 \rightarrow 3688.2} \times 100$$

$$\%error = \frac{\Delta R_{UT}}{R_{UT}} \times 100 = \frac{(-0.6\% \text{ min, } 1.17\% \text{ max})}{0,1 R_{FS}} \rightarrow \frac{(-0.06\% \text{ min, } 0.117\% \text{ max})}{R_{FS}}$$

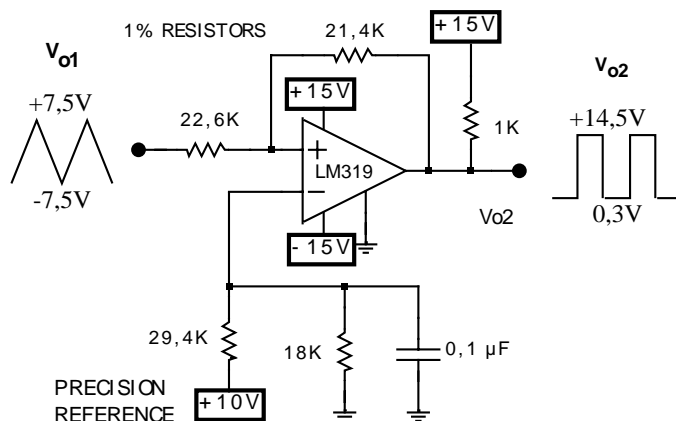
For lower resistor values the % error increases because the DC offsets are higher % wise relative to the lower voltages  $V_{RUT}$  being detected. To improve the accuracy one should use better op amps and better voltage comparators with lower DC offset voltages ( $V_{io} < 0,5 \text{ mV}$ ) this would reduce the error on the detection level to :  $HYST/2 = 2,55mV/2 = \pm 1.275mV$  or  $BIN_1 = (\pm 1,275mV/10V * 2^{12} = \pm 0,52 = \pm 0,5 \text{ LSB}$

No.7 A)

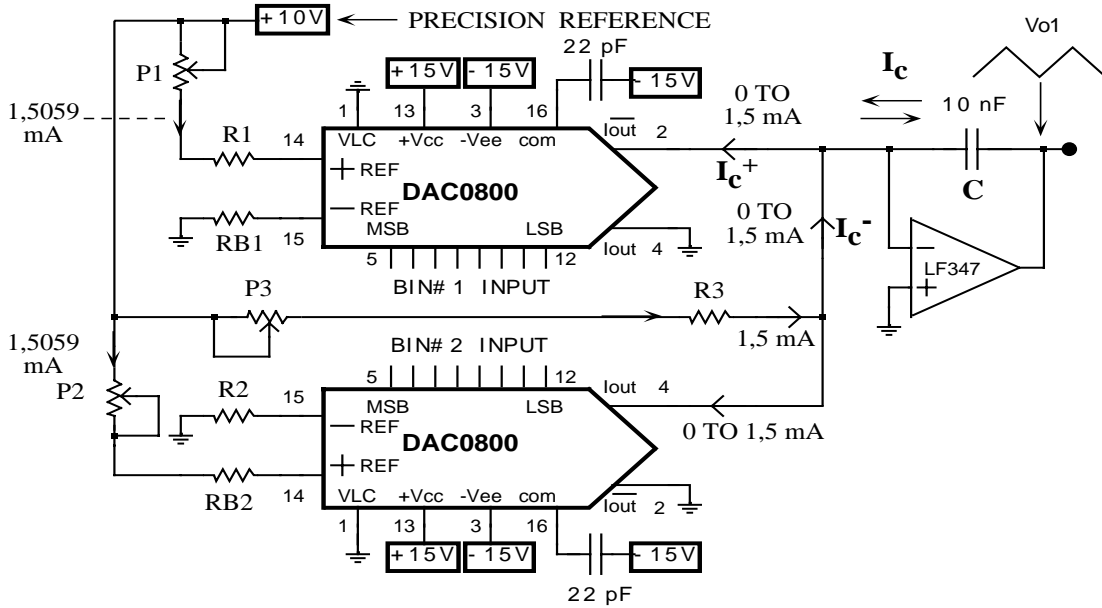
Schmitt trigger design:

Use standard design procedure.

I assumed  $V_{o2}^+ = 14,5V$  and  $V_{o2}^- = +0,3V$  for the initial design steps.



$$B) \quad \frac{\Delta V_{o1}}{\Delta t} = \frac{I_C}{C} \Rightarrow I_C = C \times \frac{\Delta V_{o1}}{\Delta t} = 10nF \times \frac{15V}{100\mu s \rightarrow \infty} = 0 \rightarrow 1,5 \text{ mA} \text{ f or } BIN = 0 \text{ to } 255$$



$R2+P2 = R1+P1 = 10V / 1.5059mA = 6641\Omega$ , use 200 $\Omega$  pot set to 100 $\Omega$  and 6541 $\Omega$  1% resistor  
 $R1+P1 = 10V / 1.50mA = 6667\Omega$ , use 200 $\Omega$  pot set to 100 $\Omega$  and 6567 $\Omega$  1% resistor

C)  $\Delta V_{o1}/\Delta t \text{ max} = 15V/100 \mu s = 150KV/s$  or  $0,15 V/\mu s \ll SR = 13 V/\mu s$  typical for LF347 therefore the op amp is fast enough.

D)

$$\frac{\Delta V_{o1}}{\Delta t} = \frac{I_C}{C} \Rightarrow \frac{\Delta V_{o1}}{PW} = \frac{I_{REF} \overline{BIN_1}}{C \times 256} \Rightarrow PW = \frac{256 \times C \times \Delta V_{o1}}{I_{REF} (255 - BIN_1)}$$

$$\frac{\Delta V_{o1}}{\Delta t} = \frac{I_C}{C} \Rightarrow \frac{\Delta V_{o1}}{SW} = \frac{1,5mA - \left( I_{REF} \times \frac{BIN_2}{256} \right)}{C} = \frac{\left( I_{REF} \times \frac{255}{256} \right) - \left( I_{REF} \times \frac{BIN_2}{256} \right)}{C}$$

$$SW = \frac{256 \times C \times \Delta V_{o1}}{I_{REF} (255 - BIN_2)}$$

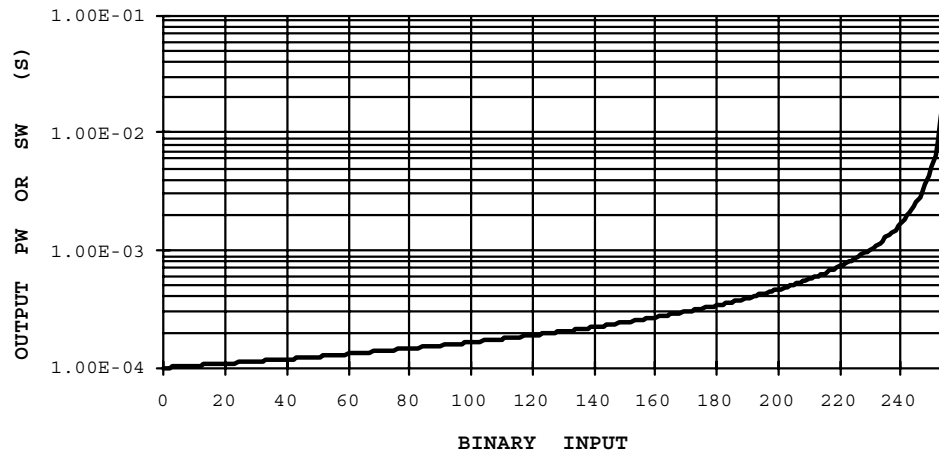
BIN	PW or SW	$\Delta PW$ or $\Delta SW$
	(s)	step size (s)
0	1.0039E-4	
1	1.0079E-4	3.9524E-7
2	1.0119E-4	3.9837E-7
3	1.0159E-4	4.0153E-7
4	1.0199E-4	4.0473E-7
-	-	-
251	6.4000E-03	
252	8.5333E-03	2.1333E-3
253	1.2800E-02	4.2667E-3
254	2.5600E-02	1.2800E-2
255	$\infty$	$\infty$

$$SW = \frac{256 \times C \times \Delta V_{o1}}{I_{REF} (255 - BIN_2)}$$

$$PW = \frac{256 \times C \times \Delta V_{o1}}{I_{REF} (255 - BIN_1)}$$

From the circuit diagram we can develop the above two equations for SW and PW and plot them on a graph as shown below. Notice that the characteristic is not linear which means that the steps (not shown) will not be constant.

PW or SW CHARACTERISTIC



No.8 A)  $V_o = 0$  to  $\pm 15,066V$  and  $\Delta V_o = 59,066$  mV

B) and D) See no 5, same modifications.