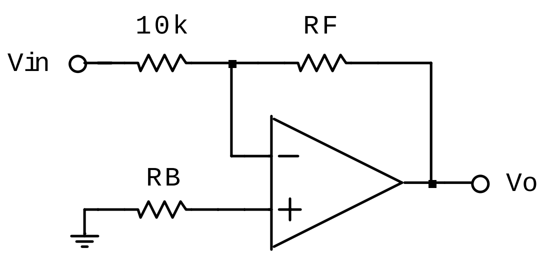
EXERCISE DC OFFSETS IN OP AMPS

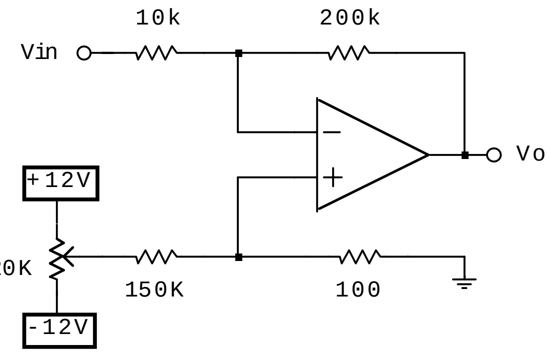
No.1 Assume an LF347 op amp.



A) What should R_B be?

B) Determine V_{oo} max for R_F values of 20K, 200K and 1M. What would you recommend for high gain circuits?

No.2 Assuming a FET input op amp, determine the range of input offset voltages that can be trimmed out by the circuit shown below.

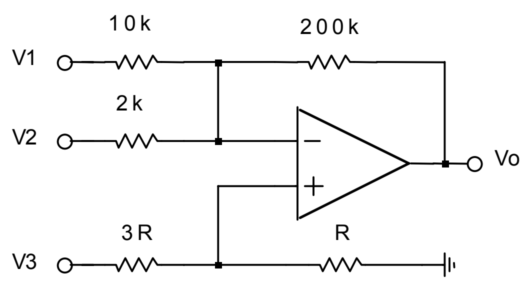


No.3 The op amp used is an OP177 from Analog Devices. Assume that I_{io} max is 40% of I_{BIAS} max specified in the data sheets.

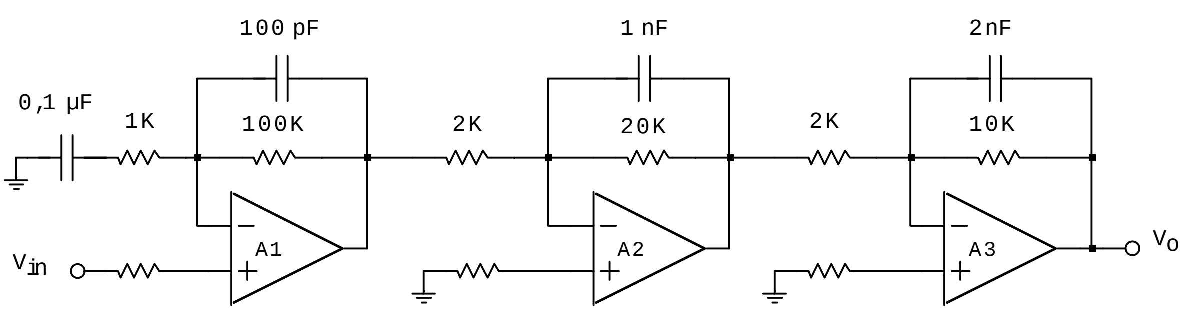
A) Determine the standard R and 3R values required to minimise the output DC offset.

B) Determine V_{OO} max assuming that the inputs are balanced.

C) Determine the drift rate of V_{oo} assuming that dI_{io}/dT is negligible.



No.4 Assume that the op amps used are AD705's from Analog Devices.



A) Determine all of the balancing resistors' standard values (5% tol).

B) Determine the optimal order of the stages and the corresponding V_{oo} max assuming that I_{io} max is 40% of I_{BIAS} max specified.

C) If the ambient temperature ranges from 0°C to +50°C, what is the maximum expected change of V_{oo}? Still assume optimum order of stages and negligible effect of dI_{io}/dT.

D) Add a balancing network to trim out V_{oo} - select proper component values. Pots available are: 10K, 20K ,50K, 100K, 200K and 500K.

SOLUTIONS

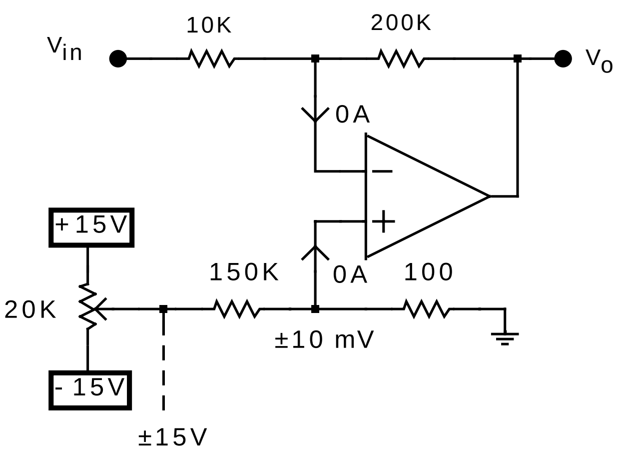
No.1 A) R_B should be zero, it is not needed with FET input op amps because the DC input bias currents are very low - xxx pA range . On the the other hand if MΩ resistors are used then one should include R_B - i.e. 100 pA x 10MΩ = 1 mV which is not negligible in high precision circuits.

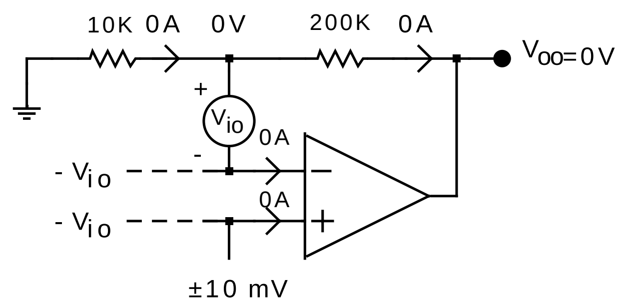
B) V_{io} max = ±13 mV max over temperature for LF347, therefore V_{oo} max = $\pm V_{io}$ $(1+R_F/R_E)$ is

V_{oo} max = ± 13m (1+(20K or 200K or 1M)/10K) = ±39 mV or ±0,273V or ±1,313V max

For high gain values ($A_{VF} = -R_F/R_E$) V_{oo} can become very large therefore a balancing network should be used if we kept using the LF347, but to avoid use of a balancing network - to avoid manual trimming of V_{oo} - one should select an op amp with a very low DC input offset.

No.2





No.3 A)

$$R_{EQ} = 2K \| 10K \| 200K = 1653 \qquad \frac{1}{R} + \frac{1}{3R} = \frac{1,3\bar{3}}{R} = \frac{1}{R_{EQ}} = \frac{1}{1653} \Rightarrow R = 2204,\ 2.2K\ std$$

3R = 3 X 2,2K = 6,6K, use 6,8K std or 6,2K + 390 if ratio is critical

NOTE: In 1% offerings there are more standard values

B)

$$R_F = 200K \qquad R_N = 2K \| 10K = 1,6\bar{6}K \qquad V_{oo} = \pm V_{io}\left(1+\frac{R_F}{R_N}\right) \pm I_{io} R_F$$

$$V_{oo} = \pm 60\mu\left(1+\frac{200K}{1,6\bar{6}K}\right) \pm (0,4 \times 2,8n \times 200K) = \pm 7,484\ mV \text{ max}$$

C)

$$\frac{dV_{oo}}{dT} = \pm\frac{dV_{io}}{dT}\left(1+\frac{R_F}{R_N}\right) \pm \frac{dI_{io}}{dT} R_F \approx \pm\frac{dV_{io}}{dT}\left(1+\frac{R_F}{R_N}\right) = \pm 1,2\,\tfrac{\mu V}{^\circ C} \times \left(1+\frac{200K}{1,6\bar{6}K}\right) = \pm 145,2\,\tfrac{\mu V}{^\circ C} \text{ max}$$

No.4 A)

$$Stage\ \ A1\quad R_B = 100K \qquad Stage\ \ A2\quad R_B = 2K\|20K = 1,82K \Rightarrow 1,8K\ std$$

$$Stage\ \ A3\quad R_B = 2K\|10K = 1,67K \Rightarrow 1,6K\ std$$

B) The optimum order for the lowest V_{oo} is **A2, A3 and A1**, that is from the highest DC gain to lowest DC gain.

From AD705 data sheets: V_{io}= 90 μV max, I_B= 0,15 nA max, assume I_{io}= 40% of 0.15n = 60 pA max

$$V_{oo} = \left(\pm V_{io2}\left(1+\frac{20k}{2k}\right) \pm I_{io2}20K\right)\times\frac{10K}{2K}\times\left(1+\frac{100K}{\infty}\right)+$$
$$\left(\pm V_{io3}\left(1+\frac{10k}{2k}\right) \pm I_{io3}10K\right)\times\left(1+\frac{100K}{\infty}\right)+$$
$$\left(\pm V_{io1}\left(1+\frac{100K}{\infty}\right) \pm I_{io1}100K\right)$$
$$V_{oo} = \pm 5,593\ \ mV \max$$

C)

$$\frac{dV_{oo}}{dT} = \pm\frac{dV_{io2}}{dT}A_{V2}A'_{V3}A_{V1} \pm \frac{dV_{io3}}{dT}A_{V3}A_{V1} \pm \frac{dV_{io1}}{dT}A_{V1}$$
$$\frac{dV_{oo}}{dT} = \pm\frac{dV_{io}}{dT}\left[A_{V2}A'_{V3}A_{V1} + A_{V3}A_{V1} + A_{V1}\right]$$
$$\frac{dV_{oo}}{dT} = \pm 1,2\tfrac{\mu V}{^oC}\left[11\times 5\times 1 + 6\times 1 + 1\right] = \pm 74,4\tfrac{\mu V}{^oC}$$
$$\Delta V_{oo\ \max} = \frac{dV_{oo}}{dT}\times\Delta T = \pm 74,4\tfrac{\mu V}{^oC}\times(50^oC - 0^oC) = \pm 3,72\ mV \max$$

D) Add balancing network to one of the inverting stages.

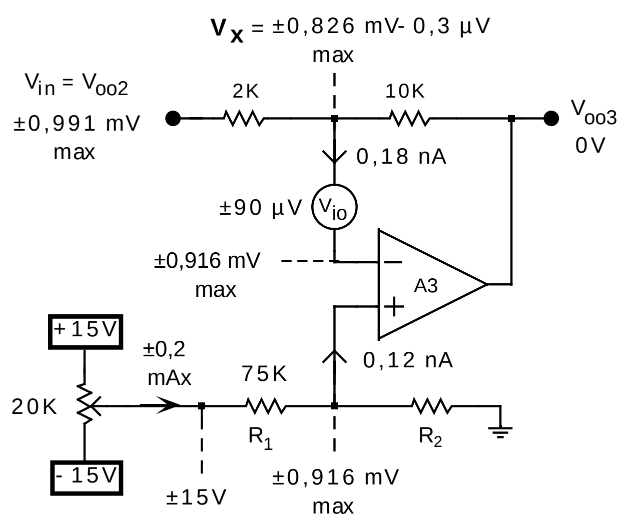
$$V_{oo2} = \pm 90\mu\left(1+\frac{20K}{2K}\right) \pm (0,4\times 0.15n\times 20K)$$
$$V_{oo2} = \pm 0,991\ mV \max$$

If I_B 0,15 nA and I_{io} = 0.06 nA, then I^+=0,18 nA and I^-=0,12 nA.

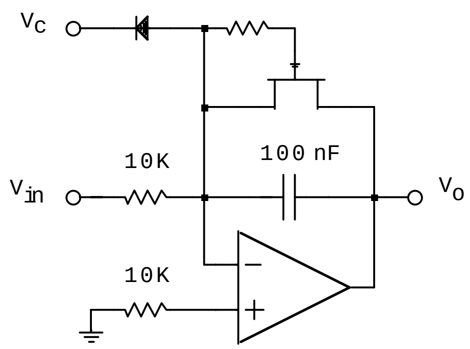
$$V'_X = -0,18n\times(2K\|10K) = -0,3\,\mu V$$
$$V''_X = \pm 0,991\ mV \times \frac{10K}{10K+2K} = \pm 0,826\ mV$$
$$V_X = V'_X + V''_X = -0,3\,\mu \pm 0,826\ m \approx \pm 0,826\ mV$$

V^+ = ±0,916 mV max, therefore let us use a ±2 mV adjustment range which makes

R_2 = 2 mV / 0,2 mA = 10Ω



No.5 **Ideal Integrator**



Op amp data: I_{BIAS}=1 nA, I_{io}=+0,1 nA, V_{io}=+1 mV

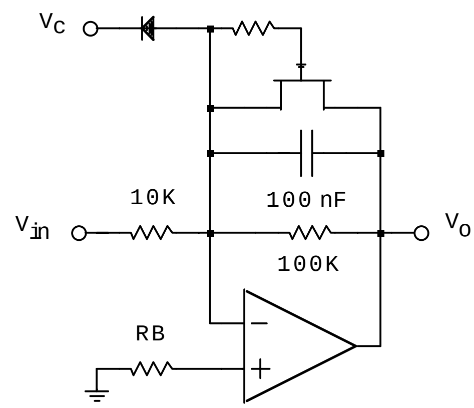
A) Assuming that the input is grounded and the FET switch is OFF, determine the small DC current running through the capacitor.

B) If the saturation voltages are ±14V, what polarity will the O/P saturate and how much time will it take to saturate?

C) If I_{io} and V_{io} are exactly zero, prove that the op amp does not saturate when the input is grounded and the FET switch is OFF.

D) What magnitude of input voltages can be integrated with less than 5% error caused by the small DC current due to I_{io} and V_{io}.

No.6 **Unideal Integrator**



Op amp data: I_{BIAS}=1 nA, I_{io}=+0,1 nA, V_{io}=+1 mV

A) A) Assuming that the input is grounded and the FET switch is OFF, determine the small DC current running through the capacitor - assuming the capacitor is initially discharged, the capacitor current will fall exponentially to zero in 5 time constants.

B) Determine the actual V_{oo} in part A after the capacitor current has reached 0A. Explain what prevents the op amp saturating when the input is grounded and the switch is OFF.