

DC OFFSETS IN OPERATIONAL AMPLIFIERS

1. Definitions

Input offset voltage (V_{io}): V_{io} is the DC differential voltage required to null the output voltage. V_{io} can be either positive or negative.

$$V_{io} = V^+ - V^- @ V_o = 0V$$

Input offset current (I_{io}): I_{io} is the DC differential current required to null the output voltage. I_{io} can be either positive or negative.

$$I_{io} = I^+ - I^- @ V_o = 0V$$

Input bias current (I_B): I_B is the average of the two input currents.

$$I_B = (I^+ + I^-)/2$$

Drift of V_{io} : rate of change of V_{io} with respect to temperature variations expressed in $\mu V/^\circ C$ or $nV/^\circ C$ - can be either +ve or -ve.

$$dV_{io}/dT$$

Drift of I_{io} : rate of change of I_{io} with respect to temperature variations expressed in $nA/^\circ C$ or $pA/^\circ C$ - can be either +ve or -ve.

$$dI_{io}/dT$$

Output offset voltage (V_{oo}): V_{oo} is a DC voltage that appears at the O/P and is a function of V_{io} , I_{io} and the resistors in the circuit. V_{oo} can be either positive or negative.

$$V_{oo}$$

2. Derivation of V_{oo}

$$I_N = \frac{0 - (-I^+ R_P - V_{io})}{R_N} = \frac{I^+ R_P + V_{io}}{R_N}$$

$$V_{oo} = -I^+ R_P - V_{io} - (I_N - I^-) R_F$$

$$V_{oo} = -I^+ R_P - V_{io} - \left(\left(\frac{I^+ R_P + V_{io}}{R_N} \right) - I^- \right) R_F$$

$$V_{oo} = -(V_{io} + I^+ R_P) \left(1 + \frac{R_F}{R_N} \right) + I^- R_F$$

$$V_{oo} = -(V_{io} + I^+ R_P) \left(1 + \frac{R_F}{R_N} \right) + (I^+ - I_{io}) R_F$$

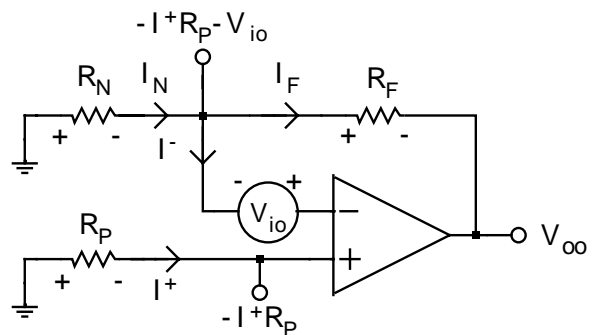
$$V_{oo} = -V_{io} \left(1 + \frac{R_F}{R_N} \right) - I^+ R_P \left(1 + \frac{R_F}{R_N} \right) + I^+ R_F - I_{io} R_F$$

The polarity of V_{io} and I_{io} is unpredictable, therefore to minimise the above expression, the second and third terms of the right expression have to cancel out:

$$I^+ R_P \left(1 + \frac{R_F}{R_N} \right) = I^+ R_F \quad \text{or} \quad R_P = R_F \parallel R_N$$

The above result shows that balancing the DC resistance seen by each input of the op amp, the DC output offset voltage V_{oo} is minimised.

General circuit



R_N : equivalent DC resistance between -ve I/P and ground.

R_P : equivalent DC resistance between +ve I/P and ground.

R_F : equivalent DC resistance between -ve I/P and O/P

I^+ and I^- : input bias currents.

Minimum DC offset	$V_{oo} = -V_{io} \left(1 + \frac{R_F}{R_N} \right) - I_{io} R_F \quad \text{if} \quad R_P = R_F \parallel R_N$
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Since the polarity of V_{io} and I_{io} can be either positive or negative, V_{oo} can also be either positive or negative. The above result also shows that V_{io} is amplified by a factor $(1+R_F/R_N)$ which is the non-inverting gain of the circuit - this means that the higher the gain, the higher V_{oo} will be.

3. FET input op amps

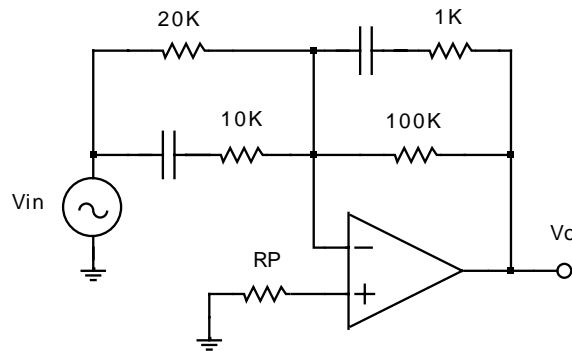
Input bias currents of FET input op amps are very small, usually in the XX pA range, therefore it is not necessary to balance the inputs for DC resistance in order to minimise V_{oo} . Making I^+ and I^- equal to zero in the above derivation, we obtain

$V_{oo} = -V_{io} \left(1 + R_F/R_N \right) \text{ for FET inputs when } I^+ \text{ and } I^- \text{ are negligible.}$

However in circuits requiring very large resistor values, it is still required to balance the inputs of FET I/P op amps for DC resistance if one wants to minimise V_{oo} . If the first term of the right member of the equation given below is too large then balancing should be used to cancel out that term to lower V_{oo} max.

$V_{oo(\max)} = I^+_{(\max)} \times \left[R_F - R_P \left(1 + \frac{R_F}{R_N} \right) \right] \pm V_{io} \left(1 + \frac{R_F}{R_N} \right) \pm I_{io} R_F$ <p style="text-align: center; margin-top: -10px;">----- first term -----</p>	where $(1 + R_F/R_N)$ is the DC gain
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Example 1



A) Determine the value of R_P required and then calculate the maximum V_{oo} if inputs are balanced and an LM741 op amp is used. Assume any temperature is possible.

$$R_P = 20K \parallel 100K = 16,7K \Rightarrow 16K \text{ std}$$

$$R_N = 20K \parallel (10K + \infty) = 20K$$

$$R_F = 100K \parallel (1K + \infty) = 100K$$

LM741 data: $V_{io} = \pm 6 \text{ mV max}$, $I_{io} = \pm 500 \text{ nA max}$

$$V_{oo} = -V_{io} \left(1 + R_F/R_N \right) - I_{io} R_F = \pm 6m \left(1 + 100K/20K \right) \pm 500n \times 100K = \pm 86 \text{ mV max}$$

B) Repeat step A with a 2M resistor instead of the 100K resistor.

$$R_p = 20K \parallel 2M = 19,8K \Rightarrow 20K \text{ std}$$

$$V_{oo} = -V_{io} (1 + R_F/R_N) - I_{io} R_F = \pm 6m(1 + 2M/20K) \pm 500n \times 2M = \pm 1,606 V \text{ max}$$

One can see that a high gain circuit produces a much larger V_{oo} which will impair the accuracy of the circuit - DC gain is $(1 + 2M/20K) = 101$ v/v here as opposed to 6 v/v in A. Another factor is the large resistor value of 2M which can contribute $\pm 500n \times 2M = \pm 1V$ max to V_{oo} . If one reduced all the resistor values by a factor of ten and multiplied all the capacitor values by a factor of ten, the circuit would perform the exact same DC and AC functions but now V_{oo} max would be smaller:

$$V_{oo} = -V_{io} (1 + R_F/R_N) - I_{io} R_F = \pm 6m(1 + 200K/2K) \pm 500n \times 200K = \pm 0,706 V$$

Now if one still needs the higher resistor values and wants the $I_{io} R_F$ term to contribute negligible voltage to V_{oo} , then the obvious choice is to use a FET input op amp. Assuming the same ± 6 mV max for a FET op amp, then V_{oo} would be:

$$V_{oo} = -V_{io} (1 + R_F/R_N) - I_{io} R_F \approx -V_{io} (1 + R_F/R_N) = \pm 6m(1 + 2M/20K) = \pm 0,606 V$$

C) Assuming a FET input op amp is used in the original circuit, determine the maximum input offset voltage required if less than 10 mV output offset must be obtained.

$$V_{oo} = -V_{io} (1 + R_F/R_N) - I_{io} R_F \approx -V_{io} (1 + R_F/R_N)$$

$$V_{io} < \frac{V_{oo \text{ max}}}{(1 + R_F/R_N)} = \frac{10m}{(1 + 100K/20K)} = 1,67 \text{ mV}$$

Example 2

A) Determine the standard values of R and 10R required to minimise the O/P DC offset.

$$R_F = 100K \quad R_p = R \parallel 10R = 0,909R$$

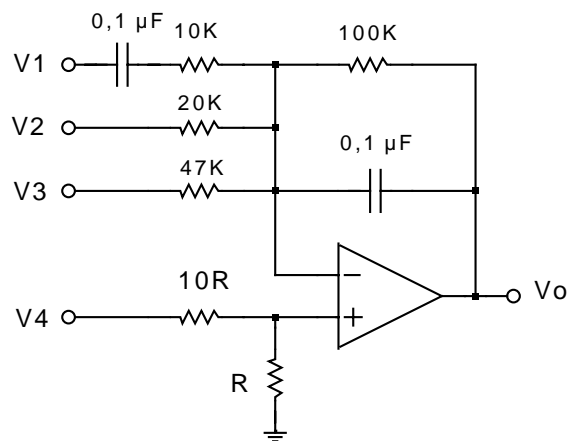
$$R_N = \infty \parallel 20K \parallel 47K = 14,03K$$

$$R_N \parallel R_F = 14,03K \parallel 100K = 12,3K$$

$$R_F \parallel R_N = R_p \Rightarrow 12,3K = 0,909R$$

$$R = 13,53K \Rightarrow 13K \text{ std}$$

$$10R = 130K \text{ std}$$



B) If an LM741 op amp is used, determine the maximum V_{oo} assuming the above R and 10R values are used.

LM741 op amp data: $V_{io} = \pm 6$ mV max, $I_{io} = \pm 500$ nA max

Inputs are balanced, therefore we have

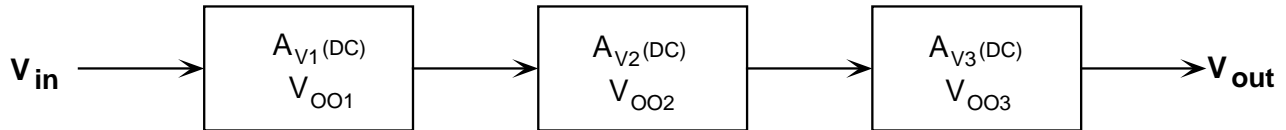
$$V_{oo} = -V_{io} (1 + R_F/R_N) - I_{io} R_F = \pm 6m(1 + 100k/14,03k) \pm 500n \times 100k = \pm 98,77 \text{ mV max}$$

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- C) Determine the maximum V_{io} required for a maximum O/P DC offset of 5 mV assuming that I_{io} max is 10 nA.

$$V_{oo} = -V_{io} \left(1 + R_F/R_N\right) - I_{io} R_F \Rightarrow V_{io \max} = \frac{V_{oo \max} - I_{io} R_F}{\left(1 + R_F/R_N\right)} = \frac{5m - 10n \times 100k}{\left(1 + 100k/14,03k\right)} = 0,492mV$$

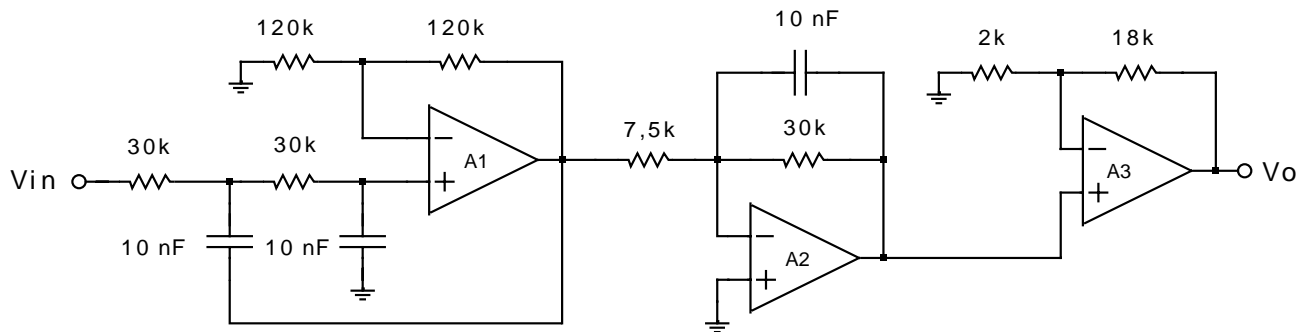
4. DC offsets in multistage circuits



$$V_{oo} = V_{oo1} A_{V2DC} A_{V3DC} + V_{oo2} A_{V3DC} + V_{oo3} \quad \text{Total output: } V_o = A_{V1} A_{V2} A_{V3} V_{in} + V_{oo}$$

The output offset of each stage is amplified by the following stage and can result in a fairly high DC offset at the final output and even saturate it if the gains are high enough - not desirable. Generally, the higher gain stages should be positioned before the lower gain stages to obtain a minimum output DC offset as will be shown in the next example.

Example



- A) Assuming that the op amps used in the above circuit have FET inputs and are all LF347's, determine the optimum order of the stages and its corresponding output DC offset.

For FET input op amps we have $V_{oo} \approx -V_{io} \left(1 + R_F/R_N\right)$ because input bias currents are very small.

The input offset voltage (V_{io}) is always amplified by the DC non-inverting gain of each stage.

$$A_1 = 1 + 120k/120k = 2 \quad A_2 = 1 + 30k/7,5k = 5 \quad A_3 = 1 + 18k/2k = 10$$

$$V_{oo} = V_{io1} A_1 A_2 A_3 + V_{io2} A_2 A_3 + V_{io3} A_3 = V_{io} \left(A_1 A_2 A_3 + A_2 A_3 + A_3\right) = A_{TOT} V_{io}$$

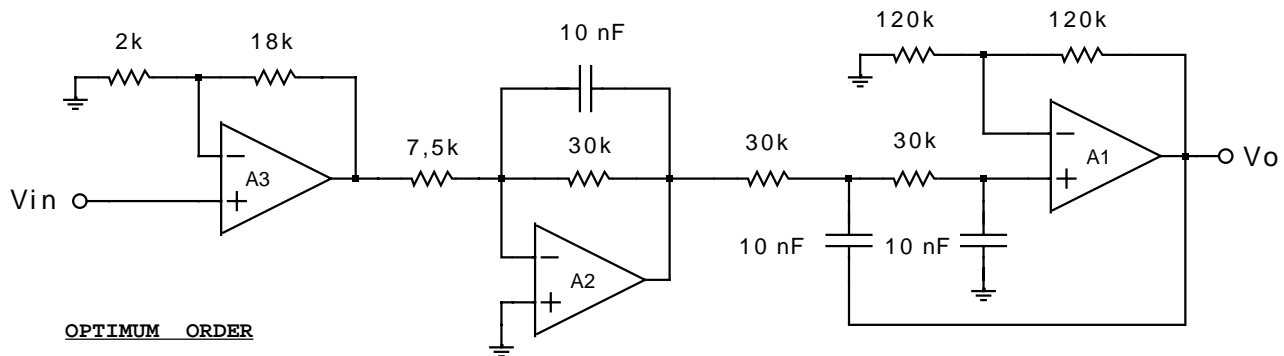
NOTE: $V_{io1 \max} = V_{io2 \max} = V_{io3 \max}$ because the same type of op amp is used in all stages.

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The order of the stages can be altered without affecting the operation of the circuit.

STAGE ORDER	1st V_{io} amplified	2nd V_{io} amplified	3rd V_{io} amplified	
	$A_{V1}A_{V2}A_{V3}$	$A_{V2}A_{V3}$	A_{V3}	A_{TOT}
1,2,3	$2*4*10=80$	$5*10=50$	10	140
1,3,2	$2*10*4=80$	$10*4=40$	5	125
2,1,3	$5*2*10=100$	$2*10=20$	10	130
2,3,1	$5*10*2=100$	$10*2=20$	2	122
3,1,2	$10*2*4=80$	$2*4=8$	5	93
3,2,1	$10*4*2=80$	$5*2=10$	2	92

From the above table one can see that the overall DC gain is minimum when the stage gains are in **decreasing order**.



$$V_{oo \max} = A_{TOT} V_{io \max} = 92 * (\pm 13\text{m}) = \pm 1,196\text{V} \max \quad \text{not too good!!!}$$

B) Determine the maximum V_{io} required if we want less than $\pm 0,1\text{V}$ DC offset at the final output and we use a different FET input op amp.

$$\text{Using the optimum order, we have } V_{io \max} = V_{oo \max} / A_{TOT} = 0,1 / 92 = \underline{1,087 \text{ mV}}$$

One has to select an op amp that meets the above constraint on $V_{io \max}$.

5. Thermal Drift of DC Offsets

I_B (input bias currents of op amp), I_{io} and V_{io} will all drift with temperature changes and this will cause V_{oo} also to drift.

$$V_{oo} \approx -V_{io} \left(1 + \frac{R_F}{R_N}\right) - I_{io} R_F \Rightarrow \frac{dV_{oo}}{dT} = -\frac{d(V_{io}(1 + R_F/R_N))}{dT} - \frac{d(I_{io} R_F)}{dT}$$

Assuming that R_F and R_N are made of the same material and dissipate little power, they will be at the same temperature and will have the same temperature coefficient. Therefore if the ambient temperature goes up and R_F goes up by 2%, R_N will also go up by the same 2% and the ratio R_F/R_N will remain constant : $1,02R_F/1,02R_N = R_F/R_N$. The term $(1+R_F/R_N)$ will be a constant and we will have the following result.

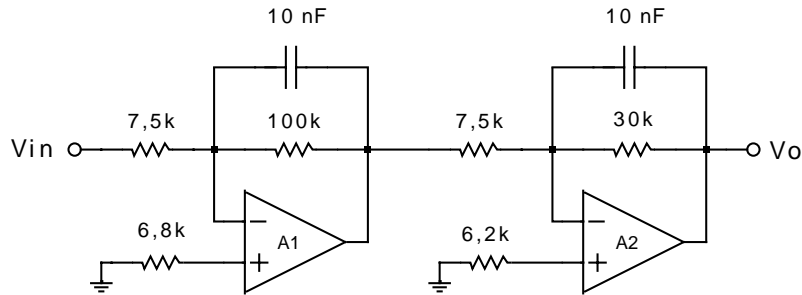
$$\frac{dV_{oo}}{dT} = -(1 + R_F/R_N) \frac{d(V_{io})}{dT} - \frac{d(I_{io} R_F)}{dT}$$

DC Offsets in Operational Amplifiers

Now if the resistors have a very low temperature coefficient, such as metal film resistors, then the resistors can be assumed constant and the drift rate becomes:

$$\frac{dV_{oo}}{dT} = -\left(1 + R_F/R_N\right) \frac{dV_{io}}{dT} - R_F \frac{dI_{io}}{dT} \quad \text{for constant resistors}$$

Example: Drift Calculations



LH0044AC OP AMP DATA

Parameter	Minimum	Typical	Maximum
Input offset voltage $T_A = 25^\circ\text{C}$, $V_{CM}=0\text{V}$, $R_S = 50\Omega$	-	8 μV	25 μV
Input offset voltage $T_{\min} < T_A < T_{\max}$, $V_{CM}=0\text{V}$, $R_S = 50\Omega$	-	-	55 μV
Input offset voltage drift $T_{\min} < T_A < T_{\max}$	-	0,1 $\mu\text{V}/^\circ\text{C}$	0,5 $\mu\text{V}/^\circ\text{C}$
Input offset current $25^\circ\text{C} < T_A < T_{\max}$	-	1,0 nA	2,5 nA
Input offset current drift $T_{\min} < T_A < T_{\max}$	-	5	40 pA/ $^\circ\text{C}$

A) Calculate the maximum V_{oo}

$$V_{oo1} = -V_{io1} \left(1 + R_F/R_N\right) - I_{io1} R_F = \pm 55\mu \times \left(1 + 100k/7,5k\right) \pm 2,5n \times 100k = \pm 788,33 \mu\text{V}$$

$$V_{oo2} = -V_{io2} \left(1 + R_F/R_N\right) - I_{io2} R_F = \pm 55\mu \times \left(1 + 30k/7,5k\right) \pm 2,5n \times 30k = \pm 350 \mu\text{V}$$

$$V_{oo(total)} = V_{oo1} A_{V2} + V_{oo2} = \pm 788,33 \mu \times \left(30k/7,5k\right) \pm 350 \mu = \underline{\underline{\pm 3,503 mV}}$$

B) Calculate the maximum drift rate of V_{oo}

$$\frac{dV_{oo1}}{dT} = \pm \left[\left(1 + 100k/7,5k\right) \times 0,5 \frac{\mu\text{V}}{^\circ\text{C}} \right] \pm \left[100k \times 40 \frac{\text{pA}}{^\circ\text{C}} \right] = 11,166 \mu\text{V}/^\circ\text{C}$$

$$\frac{dV_{oo2}}{dT} = \pm \left[\left(1 + 30k/7,5k\right) \times 0,5 \frac{\mu\text{V}}{^\circ\text{C}} \right] \pm \left[30k \times 40 \frac{\text{pA}}{^\circ\text{C}} \right] = 3,7 \mu\text{V}/^\circ\text{C}$$

$$\frac{dV_{oo}(total)}{dT} = \frac{dV_{oo1}}{dT} \times A_{V2} + \frac{dV_{oo2}}{dT} = 11,166 \mu\text{V}/^\circ\text{C} \times \left(30k/7,5k\right) + 3,7 \mu\text{V}/^\circ\text{C} = \underline{\underline{48,36 \mu\text{V}/^\circ\text{C}}}$$

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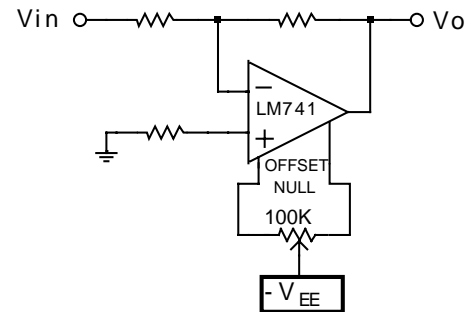
C) If we trimmed V_{oo} to exactly 0 mV at 25°C using a balancing network (see next section), what would be the maximum V_{oo} if T_A ranged from 25°C to 70 °C?

$$V_{oo \text{ max}} = \frac{dV_{oo}}{dT} (\text{max}) \times \Delta T = \pm 48,36 \mu\text{V}/^\circ\text{C} \times (70^\circ\text{C} - 25^\circ\text{C}) = \pm 2,176 \text{ mV} \quad \text{less than step A}$$

NOTE: To obtain such low DC offset voltages proper layout techniques must be used, namely guarding the op amp inputs to block out any leakage currents, and any metal-to-metal junctions of dissimilar metals will introduce a thermocouple voltage that varies with temperature and will introduce additional DC offsets therefore utmost care must be used to design all connecting points properly.

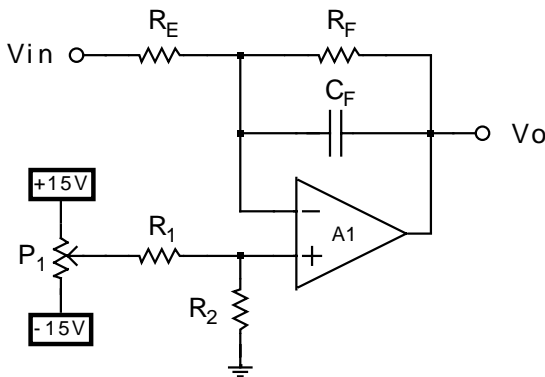
6. Balancing Networks

Balancing networks are used to null the output DC offset of op amps. Some op amp IC packages are provided with offset null pins where one can connect a few external components as shown beside for the LM741 single op amp package. The 100k potentiometer is used to unbalance the DC currents of the first stage dif amp inside the op amp thereby altering V_{oo} .

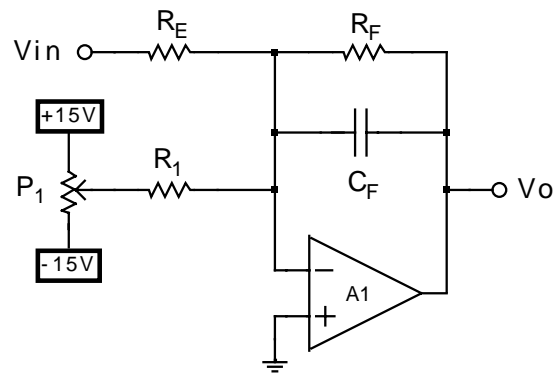


When there are no offset null pins available, one can resort to the following circuits or design his own balancing network to suit a particular application.

Inverting Circuits

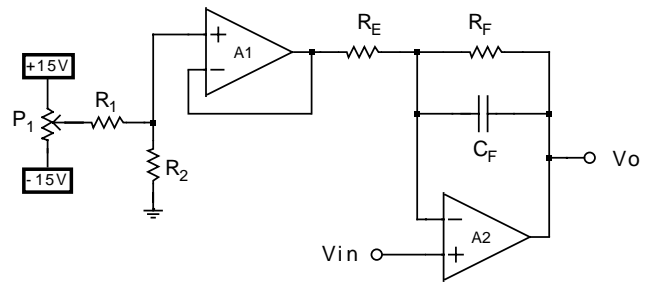
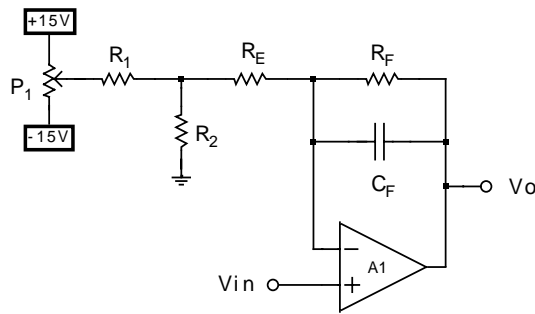


Recommended values: $R_1 = 100\text{K}$, $P_1 = 100\text{k}$ and $R_2 = 100$. Those values allow trimming of V_{io} for a range of 0 to ± 15 mV with $\pm 15\text{V}$ supplies. For less adjustment range, use a smaller R_2 value.



Recommended values: $R_1 = 1000 \cdot R_E$ and $P_1 = 100\text{k}$. Those values allow trimming of V_{io} for a range of 0 to ± 15 mV with $\pm 15\text{V}$ supplies. For less adjustment range, use a larger R_1 value.

Non-Inverting Circuits



$$A_{VF} = 1 + \frac{R_F}{R_E + R_2 \parallel [R_1 + (P_{1A} | P_{1B})]} \approx 1 + \frac{R_F}{R_E + R_2}$$

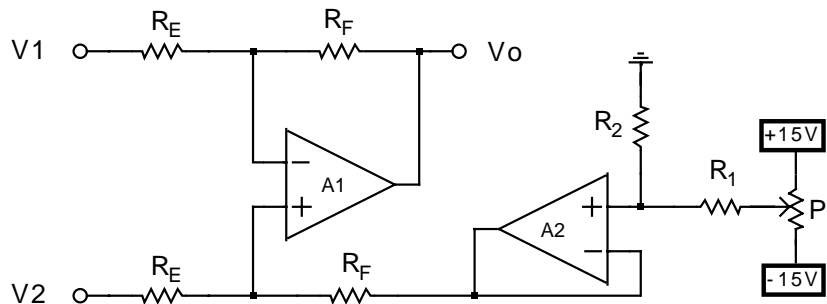
$$A_{VF} = 1 + \frac{R_F}{R_E}$$

For applications where the gain is not very critical, the above circuit can be used where it can be seen that the adjustment of P_1 will alter the gain very slightly if $R_2 \ll R_1$.

For applications where the accuracy of the gain is very critical, the above circuit provides a constant gain independent of the adjustment of P_1 .

Recommended values: $R_1 = 100K$, $P_1 = 100k$ and $R_2 = 100$. Those values allow trimming of V_{i0} for a range of 0 to ± 15 mV with $\pm 15V$ supplies. For less adjustment range, use a smaller R_2 value.

Subtractor Circuit



In a subtractor circuit the balancing network should not be connected directly to the lower R_F otherwise the CMRR of the circuit would be degraded if the R_E 's and R_F 's were initially well matched. The buffer prevents the equivalent resistance of the balancing network to add to the lower R_F and upset the match between the two R_F 's.

Recommended values: $R_1 = 100K$, $P_1 = 100k$ and $R_2 = 100$. Those values allow trimming of V_{i0} for a range of 0 to ± 15 mV with $\pm 15V$ supplies. For less adjustment range, use a smaller R_2 value.